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Multi-layer Silicon Photonic Devices for On-chip Optical Interconnects

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Multi-layer Silicon Photonic Devices for On-chip Optical Interconnects

by

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Dedication

To my family

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Multi-layer Silicon Photonic Devices for On-chip Optical Interconnects

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Supervisor: Ray T. Chen

Large on-chip bandwidths required for high performance electronic chips will render optical components essential parts of future on-chip interconnects. Silicon photonics enables highly integrated photonic integrated circuit (PIC) using CMOS compatible process. In order to maximize the bandwidth density and design flexibility of PICs, vertical integration of electronic layers and photonics layers is strongly preferred. Comparing deposited silicon, single crystalline silicon offers low material absorption loss and high carrier mobility, which are ideal for multi-layer silicon PIC.

Three different methods to build multi-layer silicon PICs based on single crystalline silicon are demonstrated in this dissertation, including double-bonded silicon-on-insulator (SOI) wafers, transfer printed silicon nanomembranes, and adhesively bonded silicon nanomembranes. 1-to-12 waveguide fanouts using multimode interference (MMI) couplers were designed, fabricated and characterized on both double-bonded SOI and transfer printed silicon nanomembrane, and the results show comparable performance to similar devices fabricated on SOI. However, both of these two methods have their limitations in optical interconnects applications.

Large and defect-free silicon nanomembrane fabricated using adhesive bonding is identified as a promising solution to build multi-layer silicon PICs. A double-layer structure constituted of vertically integrated silicon nanomembranes was demonstrated.

Subwavelength length based fiber-to-chip grating couplers were used to couple light into this new platform. Three basic building blocks of silicon photonics were designed, fabricated and characterized, including 1) inter-layer grating coupler based on subwavelength nanostructure, which has efficiency of 6.0 dB and 3 dB bandwidth of 41 nm, for light coupling between layers, 2) 1-to-32 H-tree optical distribution, which has excess loss of 2.2 dB, output uniformity of 0.72 dB and 3 dB bandwidth of 880 GHz, 3) waveguide crossing utilizing index-engineered MMI coupler, which has crossing loss of 0.019 dB, cross talk lower than -40 dB and wide transmission spectrum covering C-band and L-band.

The demonstrated integration method and silicon photonic devices can be integrated into the CMOS back-end process for clock distribution and global signaling.

Table of Contents

List of Tables

List of Figures

Chapter 1: Introduction

1.1 Introduction to silicon photonics for optical interconnects

As the scaling of microelectronics continues into nanometer range, interconnects becomes the primary limiting factor in Integrated Circuit (IC) performance. The resistive loss in electrical lines limits the bit rate on electrical lines without repeater amplifiers to $B \leqslant B_0 A/L^2$, where A is the cross-sectional area of the wiring, L is the length of the wires, and B_0 is a constant [1]. Since optics does not have this resistive loss physics limiting it, optics dominates today's long distance communication, and is considered as a promising solution to the demand for low power and high bandwidth interconnects [2]. Optical interconnects systems are emerging as alternative approaches at several levels including rack-to-rack, card-to-backplane, board-to-board, intra-board and chip-to-chip, as shown in Figure 1-1. For on-chip interconnects, Copper interconnects still dominates, and microelectronics industry are pushing the limit of copper interconnects by utilizing optimized interconnects designs, multiple interconnects layers and low-k materials. However, as the bandwidth requirement for on-chip interconnects continues to increase, the scaling of interconnects can result in increased propagation delay (ps/mm) [3]. Additionally, on-chip interconnects delay does not follow the scaling trend of transistors. As a result, the minimum achievable interconnects delay remains effectively fixed at approximately 20 ps/mm, as shown in Figure 1-2(a). To overcome the interconnects bottleneck in future electronic chips, optical interconnects becomes a promising solution by replacing electrical wires with fast optical waveguides, as shown in Figure 1-2(b).

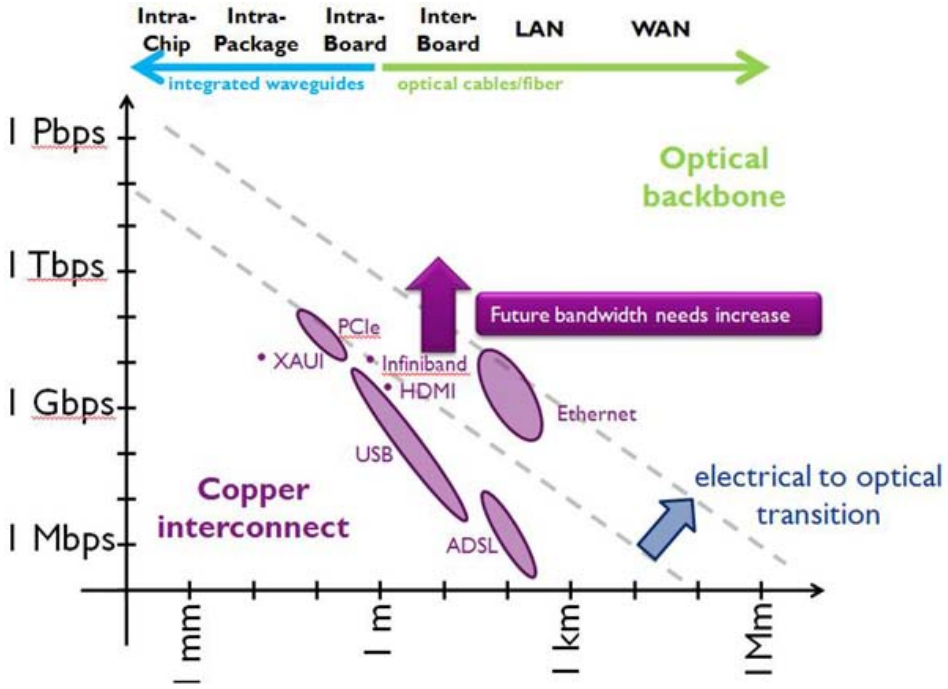

Figure 1-1: Bandwidth x distance applications requirements for short and long distance communication links [4].

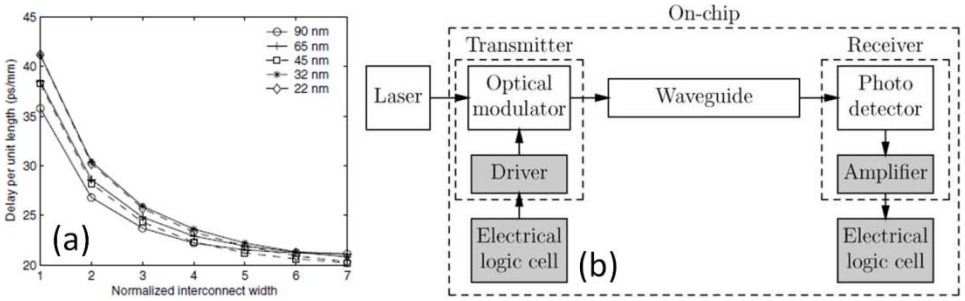

Figure 1-2: (a) Propagation delay of electrical interconnects at different technology nodes versus normalized interconnects width, (b) block diagram of the optical interconnects system [3].

On-chip optical interconnects offers potential bandwidth density advantage comparing to electrical interconnects, because wavelength-parallel signals can be transmitted through optical waveguides using wavelength-division multiplexing (WDM), as well as potential delay advantage, because the delay in optical interconnects is only

related to the effective refractive index of the waveguides. Silicon has long been the fundamental material in microelectronics. Silicon photonics, which enables monolithic integration of optical interconnects into microelectronic chips, has received worldwide interest for its potential application in on-chip optical interconnects [5]. Silicon has a high refractive index of ~3.47, which provide high refractive index contrast to cladding materials such as silicon oxide (n=1.45). This high refractive index contrast enables tight confinement of optical mode in submicron silicon waveguides, which provides high bandwidth density (Gbs/μm) in optical interconnects. (Bandwidth density is defined as $BW=D/(t_{clk}P)$, where t_{clk} is the clock period, D is the die size, and p is the pitch [2]. The pitch is defined as the necessary spacing between two waveguides to avoid crosstalk.) Figure 1-3(a) shows a cross-sectional scanning electron microscope (SEM) image of a typical silicon single-mode waveguide, which has a cross-sectional dimension of 500 nm x 250 nm. The transverse-electric (TE) optical mode in the silicon single-mode waveguide is shown in Figure 1-3(b). Note that the optical mode in the silicon single-mode waveguide is overlapped with the sidewalls of the waveguide. The scattering at the sidewalls is the primary reason for loss in such submicron waveguide. Moreover, wavelength-division-multiplexing (WDM) technology can be utilized to further increase the bandwidth density of an optical interconnects system. Transmission of a 1.28-Tb/s data stream (32 wavelengths x 40-Gb/s) through a silicon single-mode waveguide has been demonstrated in [6]. Considering the potential advantages in delay and bandwidth density, silicon photonics is considered a promising solution to on-chip optical interconnects, not to mention its compatibility with current complementary-metal-oxide-semiconductor (CMOS) process.

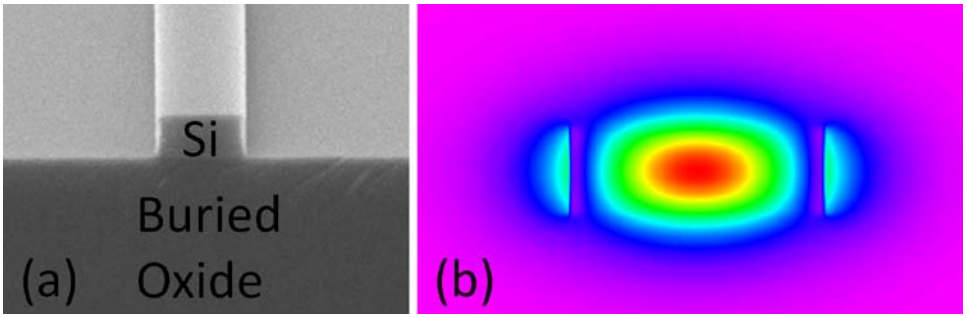

Figure 1-3: (a) A cross-sectional SEM image of a silicon single-mode waveguide with air cladding, (b) mode profile of TE fundamental mode in a silicon single-mode waveguide.

3D SILICON PHOTONICS USING DEPOSITABLE APPROACHES

To date, most silicon photonic devices, including waveguides, couplers, modulators and detectors, are demonstrated on the silicon-on-insulator (SOI) platform [7, 8]. In 2012, IBM announced 90nm silicon photonic integrated circuit, which has been verified in a manufacturing environment [9], as shown in Figure 1-4(a). In this PIC, silicon nanophotonics circuits, including modulators, waveguides and photodetectors, are fabricated side-by-side with silicon transistors. This front-end silicon photonic integration method allows high-performance photonic devices fabricated on single crystalline silicon, and seamless use of W plugs and M1 Cu metal, which benefit significantly from standard CMOS processing. However, considering the minimum spacing between optical waveguides to avoid crosstalk, which can not be scaled, and the relatively large sizes of on-chip photonic components, such as low-loss waveguide crossings and beam splitters [10, 11], the bandwidth density of single-layer silicon photonic chips is still limited comparing to the scaled electrical interconnects. Moreover, a single-layer SOI platform limits the photonic devices to the electronic layer. Silicon photonics requires a thick buried oxide (BOX) layer of 1-3μm for optical isolation from the substrate, but electronics requires an ultra-thin BOX layer for device performance consideration.

Vertical integration of multiple photonic and electronic layers can ameliorate the limited bandwidth density on a single layer PIC, and provide more design flexibility in the system design, as the photonics and electronics can be separated [12].

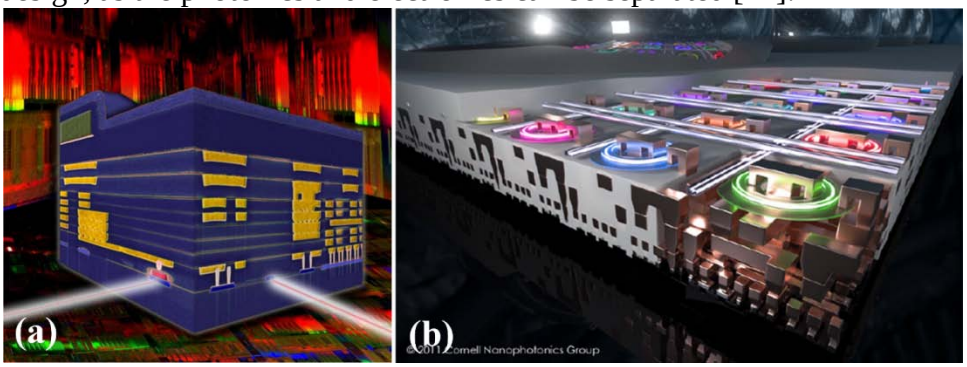

Figure 1-4: (a) IBM's front-end integrated silicon PIC (red: photodetector, blue: modulator, yellow: metal line), (b) Cornell's vision of a 3D optical network on a microelectronic chip based on deposited optics over CMOS electronics [9, 13].

In order to build a multi-layer PIC, CMOS compatible silicon deposition methods, which can be integrated into CMOS back-end process, are strongly desired, as shown in Figure 1-4(b). This method decouples photonics from the sensitive front-end process, and alleviates the stringent footprint requirement of photonic devices [14]. Multi-layer silicon photonic platforms have been demonstrated with film deposition approaches, including hydrogenated amorphous silicon and silicon nitride deposited by plasma-enhance chemical vapor deposition (PECVD) [13, 15]. Hydrogenated amorphous silicon is a low-loss material for waveguiding. However, sufficient and stable hydrogenation of the silicon dangling bonds is critical to maintain its low-loss property. Zhu et al have demonstrated that the propagation loss for hydrogenated amorphous silicon waveguides are sensitive to process temperature and cladding materials [16], and Selvaraja et al have shown that the refractive index change measured from a Mach-Zehnder Interferometer (MZI) starts to occur at 200°C [17]. In addition to thermal stability of hydrogenated

amorphous silicon, another significant challenge is that the charge mobility is very low due to the amorphous structure of the film, thereby limiting its application in high-speed applications. Silicon nitride is another low loss material for waveguiding, but its lower index comparing to silicon increases device footprint, and it also lacks any mechanism for high-speed modulation, limiting nitride to either passive devices or slower devices using the thermo-optic (TO) effect.

Polycrystalline silicon is another depositable material considered to build multi-layer silicon PICs [18]. Although some important devices such as high quality factor ring resonators [18], and high speed electro-optic modulators [19] have been demonstrated, one fundamental issue about polycrystalline silicon is its material loss. One primary source for loss in polycrystalline silicon is the absorbing and scattering at grain boundaries inside poly crystalline silicon. In order to reduce such grain boundary induced loss, solid phase crystallization (SPC) of low pressure chemical vapor deposition (LPCVD) amorphous silicon is used as the method to fabricate polycrystalline silicon layers for photonic application instead of direct deposition of LPCVD polycrystalline silicon [20]. The SPC process requires a temperature of ~1000°C, which is not compatible with the CMOS backend process. Even with the SPC process, the lowest propagation loss of a single-mode polycrystalline silicon waveguide demonstrated so far is 6.45 dB/cm [21], which is much higher than that of a single-mode crystalline silicon waveguide. Kwong et al demonstrated single-mode polycrystalline silicon waveguides using the processing equipments in UT-Austin Microelectronic Research Center, as shown in Figure 1-5. Grain sizes of ~300 nm is clearly shown in Figure 1-5(a), which is one of the key reasons for waveguide propagation loss in polycrystalline silicon waveguides. Polycrystalline silicon single-mode waveguides, with a cross-sectional dimensions of 500 nm X 250 nm, as shown in Figure 1-5(b), has a propagation loss

of >15 dB/cm [20], which is too high to be used in large-scale PIC, not to mention its thermal incompatibility with CMOS back-end process.

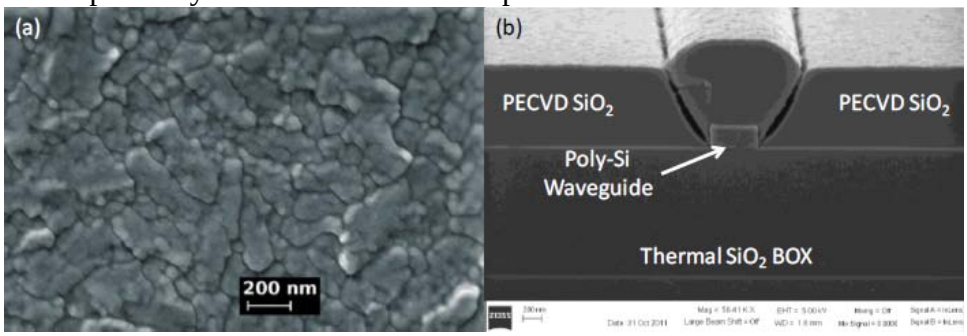

Figure 1-5: (a) Top-down SEM image of polycrystalline silicon grains after oxidation and buffered oxide etching (BOE), (b) cross-sectional SEM image of a single-mode polycrystalline silicon waveguide [20].

In order to investigate the feasibility to build multi-layer silicon photonic structures using depositable approaches with the processing equipments in UT-Austin Microelectronic Research Center, I fabricated a double-layer waveguide structure by depositing 250 nm thick hydrogenated amorphous silicon layer on top of waveguides fabricated on single-layer SOI, with 2 μm PECVD oxide in between for optical isolation. The recipe used to deposit amorphous silicon can be found in ref. [22]. Waveguides on the amorphous silicon layer were fabricated using electron beam lithography (EBL) and reactive ion etching (RIE). The input waveguide is 2.5 μm wide, which matches the mode field diameter of a lensed fiber. This is tapered down to a single mode width of 500 nm using a 500μm long linear taper after an S-bend structure. Optical testing was performed on a six-axis automated aligner system with a 50 nm precision in movement. A lensed polarization maintaining fiber (PMF) with a 2.5 μm output mode diameter was used to couple TE polarized light at 1550 nm into the input waveguide. The light's propagation through the amorphous silicon waveguide was recorded with an IR-CCD camera mounted on top of the device under testing, as shown in Figure 1-6(a). As we can see, the

light trail diminishes very fast after the S-bend, meaning the single-mode waveguide fabricated on amorphous silicon has significant propagation loss. Comparing with an IR-image showing light's propagation through an amorphous silicon waveguide fabricated directly on top of a thermal oxide layer on a silicon wafer, as shown in Figure 1-6(b), we conclude that the deposited PECVD oxide layer will bring significant additional loss to the waveguides fabricated on top of it. A cross-sectional SEM image of the double-layer waveguiding structure at the input end is shown in Figure 1-6(c). Obvious roughness at the top and bottom surfaces of the deposited amorphous silicon layer is observed, which is the main reason for the additional loss. This surface roughness will also be presented in silicon nitride layer deposited on top of a PECVD oxide layer. Although this problem can be solved by chemical mechanical polishing (CMP), it is beyond the ability of our fabrication facilities. Moreover, we found that both the refractive index and the propagation loss are dependent on the hydrogen concentration in the amorphous silicon layer, which is not stable for long term consideration.

Recent efforts in building deposited multi-layer photonic platform combine the use of polycrystalline silicon and silicon nitride [14, 23]. Polycrystalline silicon can be used to build active photonic devices and silicon nitride can be used to build low-loss waveguides. However, in order to be compatible with CMOS back-end thermal budget, large-grain polycrystalline silicon can only be formed by low-temperature excimer-laser-annealing (ELA), not by high-temperature annealing in furnace. To date, no promising device has been demonstrated using ELA polycrystalline silicon. Moreover, single-mode waveguides fabricated using as-deposited silicon nitride shows ~6 dB/cm propagation loss in C-band [13], which is worse than state-of-art single-mode waveguides fabricated on single crystalline silicon. In order to achieve ultra-low loss property in silicon nitride,

high temperature annealing is required, which is not compatible with CMOS back-end process.

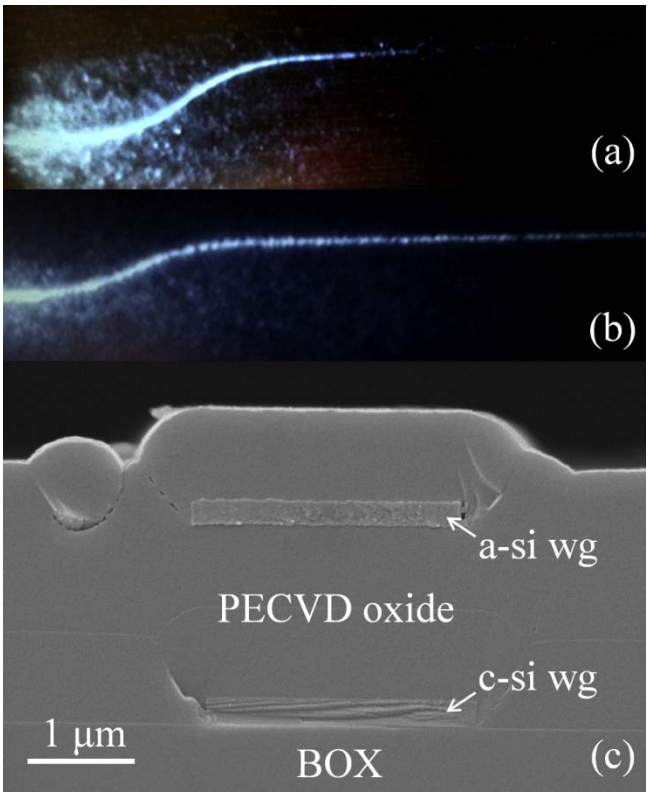

Figure 1-6: (a) Top-down IR image showing light propagating in amorphous silicon waveguide fabricated on PECVD oxide layer, (b) top-down IR image showing light propagating in amorphous silicon waveguide fabricated on thermal oxide layer, (c) cross-sectional SEM image of the double-layer waveguiding structure using deposited amorphous silicon on SOI.

3D SILICON PHOTONICS USING SINGLE CRYSTALLINE SILICON

Single crystalline silicon is the most desirable material for multi-layer silicon PICs due to its superior materials such as low material absorption loss and high carrier mobility. Utilizing single crystalline silicon as additional photonic layers also enables direct use of state-of-art silicon photonic devices demonstrated on SOI in 3D integration without re-optimizing devices for deposited silicon layers. As it is not currently possible

to deposit single crystalline silicon, other approaches need to be investigated to build multi-layer structures comprised of single crystalline silicon. The investigation of approaches to build single crystalline silicon based multi-layer silicon PICs and the demonstration of novel silicon photonic devices that enable 3D integration of silicon photonics are the primary goals of my dissertation.

DISSERTATION ORGANIZATION

This dissertation is arranged as follows:

In chapter 1, recent developments in silicon photonics for on-chip optical interconnects are reviewed. The depostitable approaches to build multi-layer silicon PIC and their limitations are summarized. Our efforts to build deposited multi-layer silicon PIC are briefly described and our vision to build multi-layer PIC using single crystalline silicon is proposed.

In chapter 2, double-layer silicon photonic devices fabricated on double-bonded SOI are demonstrated. We developed a deep reactive ion etching process to fabricated self-aligned waveguiding structures on double-bonded SOI. Double-layer multimode interference (MMI) coupler was designed, fabricated and characterized. Experimental results revealed that the device performance was comparable to similar device fabricated on SOI.

In chapter 3, double-layer silicon photonic devices integrated using transfer-printing techniques are demonstrated. Large-area transferrable silicon nanomembranes were fabricated in University of Illinois at Urbana-Champaign and transfer printed onto single-layer silicon PIC fabricated in UT-Austin. We developed a fabrication process for fabricating silicon photonic devices on transfer-printed silicon nanomembranes. Double-

layer MMI coupler was designed, fabricated and characterized. The feasibility to use transfer printed silicon nanomembrane in multi-layer PIC was evaluated.

In chapter 4, intra- and inter-layer grating couplers based on subwavelength nanostructure are demonstrated on multi-layer silicon nanomembrane platform. The principle of subwavelength nanostructure and the design of grating couplers for both fiber-to-chip coupling and on-chip inter-layer coupling were presented. Vertically integrated double-layer silicon nanomembranes were fabricated using SU-8 adhesive bonding and silicon handle etch-back processes. Experimental characterizations show promising results for grating coupler's applications in 3D integration of silicon photonics.

In chapter 5, 1-to-32 H-tree optical distribution is demonstrated on adhesively bonded silicon nanomembrane. The loss of the H-tree optical distribution was thoroughly characterized and the results show comparable performance to similar structures fabricated on SOI.

In chapter 6, ultra-low loss waveguide crossing is demonstrated using cascaded index-engineered MMI structures. The loss mechanism in MMI based waveguide crossings was thoroughly investigated. Large-scale cross-grid constituted of MMI based waveguide crossings index-engineered using subwavelength nanostructures were designed, fabricated and characterized. Experimental results confirmed our theoretical analysis and showed ultra-low insertion loss and low cross-talk for our crossings.

In chapter 7, the dissertation is summarized and potential future works are suggested.

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Chapter 2: Vertically Integrated Double-layer On-chip Silicon Membranes for 1-to-12 Waveguide Fanouts

INTRODUCTION

Large on- and off-chip bandwidths required for high performance multi-core structures (~10 TB/s by 2015) corresponding to interconnect energy budgets of ~100 fJ/bit will render optical components essential parts of future high performance integrated systems [1-3]. CMOS compatible silicon photonics, which allows for integration of optical components on the same silicon chip with CMOS transistors, is considered one of the solutions to such a high demand for low energy and high bandwidth communications [3, 4]. Since the Luxtera silicon photonic chip in 2002, the number of on-chip photonic components has doubled each year [5, 6]. There is also a "Moore's law like" trend observed in InP-based PIC development since 1988 [7]. However, due to the large sizes of the on-chip photonic components, single layer photonic component counts cannot exceed 1000 and 10,000 in InP and silicon PICs, respectively [8]. As discussed in chapter 1, vertical integration of multiple layers of active and passive components can resolve the problem of limited real estate on a single layer. So far, single crystalline silicon remains the best material for silicon photonics. Commercially available SOI wafers are the primary platform for silicon photonics, on which 1 dB/cm to 2 dB/cm propagation loss have been demonstrated for silicon single-mode waveguides [9, 10].

In this chapter, we demonstrate a 3D photonic integration of self-aligned structures using double-bonded SOI wafers by fabricating double-layer 1x12 multimode interference (MMI) couplers on silicon membranes. Using the presented scheme, multi-levels of PICs including waveguide arrays, MxN MMI couplers, and arrayed waveguide gratings (AWGs) can be vertically integrated to significantly increase the on-chip integrated photonic component count.

DEVICE DESIGN

The schematic of a 1xN MMI coupler is shown in Figure 2-1(a), where W_w is the width of the input and output access waveguides' width, W_{MMI} is the width of the MMI, L_{MMI} is the length of the MMI and N is the number of outputs. W_e is the effective width of the MMI, which includes the optical modes penetrate out the MMI region. For silicon photonics, which has a tight mode confinement due to the high index contrast between silicon and cladding materials, $W_e=W_{MMI}$ can be used for MMI design. The schematic of the double-bonded SOI wafer and self-aligned waveguide structure are shown in Figure 2-1(b). The thicknesses of both silicon layers are h1=h2=1.3μm, and the two BOX layers are both 2.0μm thick.

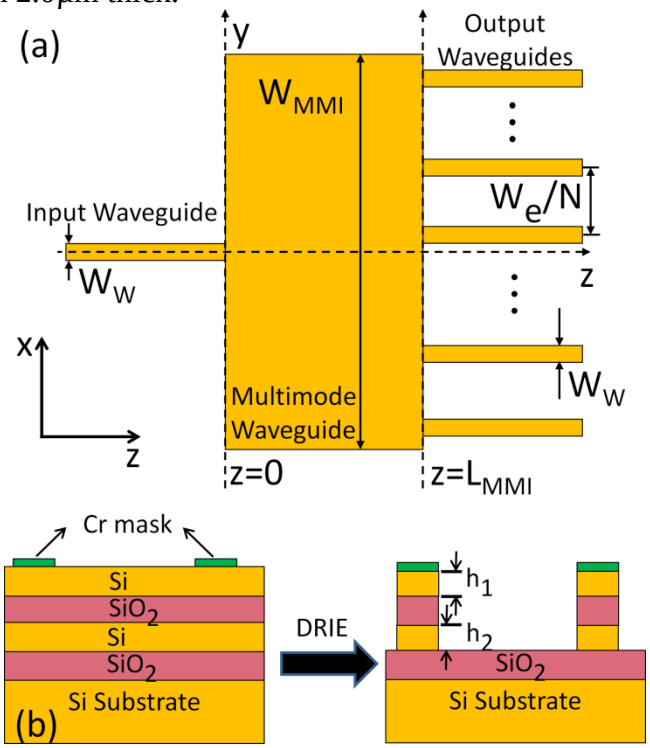

Figure 2-1: (a) A schematic of 1xN MMI coupler, (b) a schematic of the double-bonded SOI wafer and the fabrication process to form self-aligned waveguides.

We choose W_{MMI}=60 μm. The MMI length with a 1xN fanout is given as $L_{MMI} = (n_{eff} W_{MMI}^2)/(\lambda_0 N)$ =664 μm [11], where n_{eff}=3.43 (for 1.3 μm thick silicon membrane) is the effective refractive index of the TE fundamental mode of the multimode waveguide, and λ_0=1.55 μm is the free space wavelength. W_w=2.5 μm matches the mode sizes of the input/output lensed fibers. Thus, the fiber-waveguide coupling tolerance is enhanced due to the waveguides' relatively large end-fire cross sections. The simulated MMI performance using FIMMPROP based on eigenmode expansion is shown in Figure 2-2. The simulated effective index of the fundamental TE and transverse magnetic (TM) modes in the access waveguides are 3.417 and 3.412, respectively, at λ=1.55 μm. Polarization independent operation is expected due to the small difference between the TE and TM effective indices. MMI couplers can be used for efficient on-chip beam splitting [11]. A complete analysis for a symmetrically excited 1xN MMI coupler with uniform output was presented in Ref. [12]. We fabricate two self-aligned 1x12 MMI couplers on two vertically stacked silicon membrane layers using one lithography process followed by a single etching step, as described in the device fabrication part below.

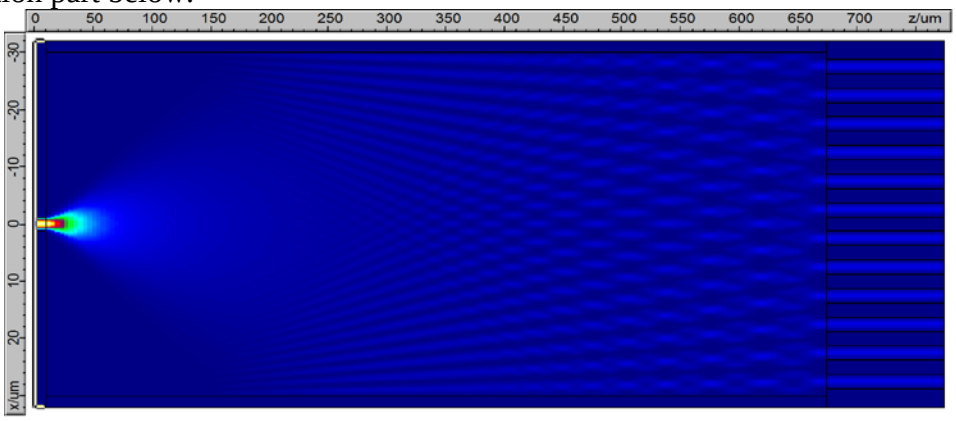

Figure 2-2: Simulated MMI performance using FIMMPROP.

DEVICE FABRICATION

The double-bounded SOI wafers are fabricated using fusion bonding and etch-back [13], and are commercially available from Ultrasil. A 100 nm thick chromium etching mask is defined through an electron beam lithography (EBL) and lift-off process. The pattern is then transferred to both silicon layers using one SF_6/C_4F_8/Ar based Deep Reactive-Ion-Etching (DRIE) step in Plasma-Therm's Versaline system. The DRIE process consists of ~1000 iterations of a two-step polymer deposition/etching cycle. Afterwards, the chromium mask is removed with wet etching. The sidewall profile control in the DRIE process is the key to the performance of the fabricated devices. Although the Bosch process based DRIE of silicon, which alternates repeatedly between deposition of a polymer passive layer and isotropic plasma etching of silicon, is well developed in industry [14] and the standard recipes are provided by the system manufacturer, it has a very slow etch rate for silicon oxide and is not applicable for etching into double-bonded SOI wafers. In order to achieve a vertical sidewall, several process parameters need to be optimized, including gas composition, bias radio frequency (RF) voltage, inductively coupled plasma (ICP) power, chamber pressure, and step time. A standard recipe (Table 2-1) for etching SOI wafers is used as the base recipe for parameter optimization. Wafer loading and temperature are kept constant during the optimization process.

Table 2-1: DRIE base and final parameters for one deposition and etching cycle.

Steps	Gas flow rate (sccm)						Bias RF voltage (V)		ICP power (W)		Pressure (mTorr)		Time (s)	
	SF6		C4F8		Ar									
	Base	Final	Base	Final	Base	Final	Base	Final	Base	Final	Base	Final	Base	Final
Deposition	50	50	125	125	10	10	10	10	1600	1600	20	20	0.8	0.8
Etching	60	50	40	40	10	10	250	400	1200	1500	20	20	2	2

We have done a thorough investigation on the effects of different parameters in the DRIE process, as summarized below:

1) Decreasing C_4F_8 gas flow rate and ICP power during the deposition step results in the decrease of polymer deposition rate. This generally results in faster etch rate but less sidewall protection. However, we found that increasing C_4F_8 gas flow rate and ICP power beyond 125sccm and 1600W will not result in less undercut. This is due to the increase of total cycles required at a slower etch rate. As discussed in reference [15], the undercut to the top silicon layer will be more severe as total etching time increases, due to the decrease of polymer deposition rate on the sidewall when the silicon etch front starts to undercut the mask.

2) Increasing SF_6 gas flow rate and ICP power during the etching step results in more isotropic etching of the silicon photonic layer. While this can provide a faster etch rate, it is ultimately detrimental in that it causes more damage to the polymer layer on the sidewall.

3) Decreasing step time in the etching step results in less damage to polymer layer on the sidewall, but also increases the total cycles required to etch the double-layer structure. As discussed in reference [15], the undercut to the top silicon layer will be more severe as total etching time increases, due to the decrease of polymer deposition rate on the sidewall when the silicon etch front starts to undercut the mask. We found that decreasing etching step time beyond 2s will not result in less undercut.

4) Chamber pressure is kept same for both deposition and etching steps during the whole etching process. Decreasing pressure results in the decrease of polymer deposition rate and an increase of etch anisotropy.

5) Increasing bias RF voltage in the etching step generally results in faster etch rate in vertical direction, but also results in significant isotropic etching of silicon photonic layer when beyond 400V.

By individually optimizing these parameters to achieve vertical sidewalls, we arrive at the final recipe, which is also shown in Table 2-1. We determine that the bias RF voltage has the largest impact on the anisotropy of the sidewall profile. A larger bias RF voltage results in a higher etch rate and yields a more vertical sidewall profile during silicon oxide etching, but it also causes more damage to the polymer layer on the sidewall of the silicon membrane layer. Figure 2-3(a) shows the cross section of a waveguide etched using our otherwise final recipe with a 450 V bias RF voltage. The polymer layer on the sidewall is consumed the etching step and results in a large undercut to the top silicon layer, leading to significant deviation from the original design. Figure 2-3(b) shows the cross section of a waveguide etched using the final recipe. The result shows a reduced undercut and a ~80° tapered sidewall profile during the silicon oxide etching. The undercut to the top silicon layer is inevitable due to the required ~40 minute etch time of the BOX layer [15].

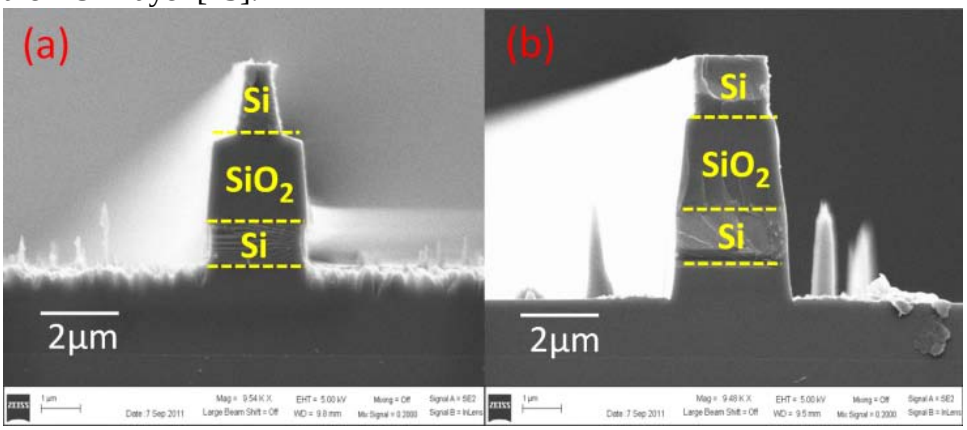

Figure 2-3: SEM images of the waveguide cross section under different etching conditions, (a) a waveguide cross section with large undercut, (b) a waveguide cross section with corrected undercut.

The fabricated MMI access waveguides are 2.0 µm and 2.9 µm wide on the top and bottom layers, respectively. These access guides also correspond to TE fundamental mode effective refractive indices of 3.410 and 3.419, respectively, as shown in Figure 2-4. We note that because of the large thicknesses of the silicon layers, the effective index changes negligibly with variations in the waveguide width.

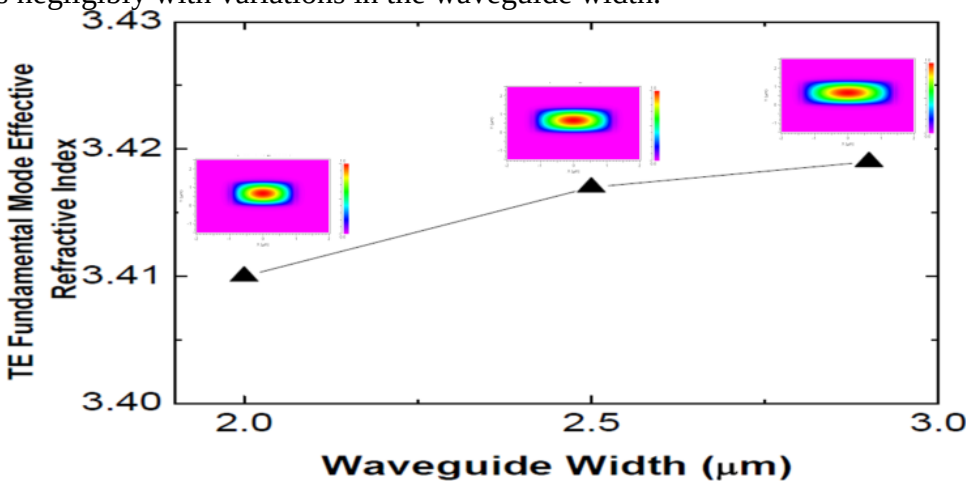

Figure 2-4: TE fundamental mode profiles and effective refractive indices at different waveguide widths.

Figure 2-5(a) shows a microscope image of the overall double-layer MMI. Figures 2-5(b) and 2-5(c) show the scanning electron microscope (SEM) images of the MMI output region and the output facet, respectively, with their corresponding locations labeled in Figure 2-5(a).

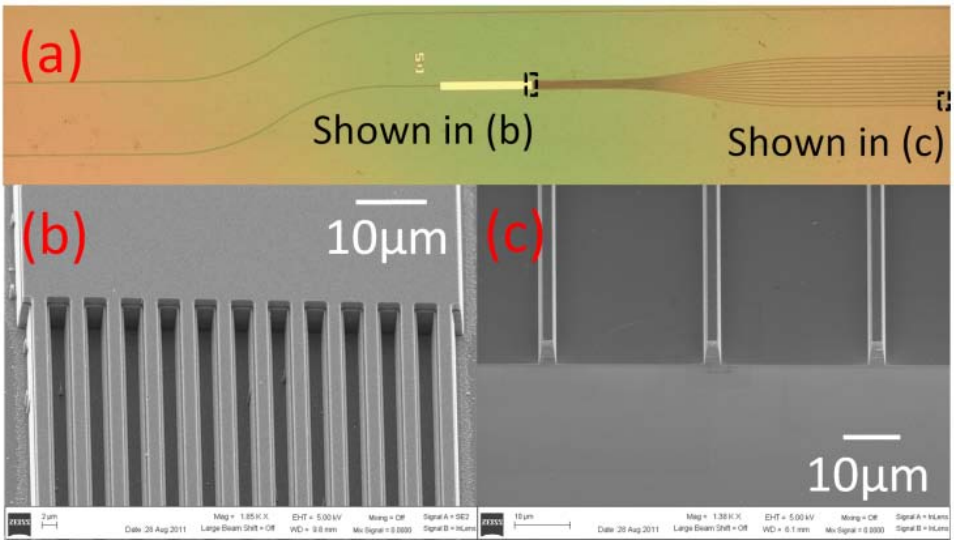

Figure 2-5: (a) Optical microscope image of the double-layer MMI, (b) SEM image of the MMI output region, (c) SEM image of the output waveguide's facet.

DEVICE CHARACTERIZATION

A six-axis automated aligner system with a movement precision of 50 nm is utilized to couple TE polarized light at a wavelength of 1550 nm from a polarization maintaining lensed fiber (PMF) with a 2.5 µm output mode diameter into the silicon waveguide inputs. An infrared (IR) camera connected to a variable objective lens captures the top-down, near-field images of the output facets. In order to visually resolve the 12 output spots, a waveguide fanout design is used to increase the separation of each adjacent channel to 30 µm [Figure 2-5(c)]. In order to visualize individual layer coupling in our double-layer device, we separate the outputs in the bottom layer from those in the top layer so that the two device layers terminate at two different locations as shown in Figure 2-6(a). Figures 2-6(b) and 2-6(c) illustrate the excitation of top and bottom layer MMI couplers, respectively. These results demonstrate selective coupling to each layer with negligible crosstalk, which in turn is due to the 2 µm thick BOX layer between the

two silicon layers. Figure 2-6(d) illustrates the simultaneous excitation of top and bottom layer MMI couplers.

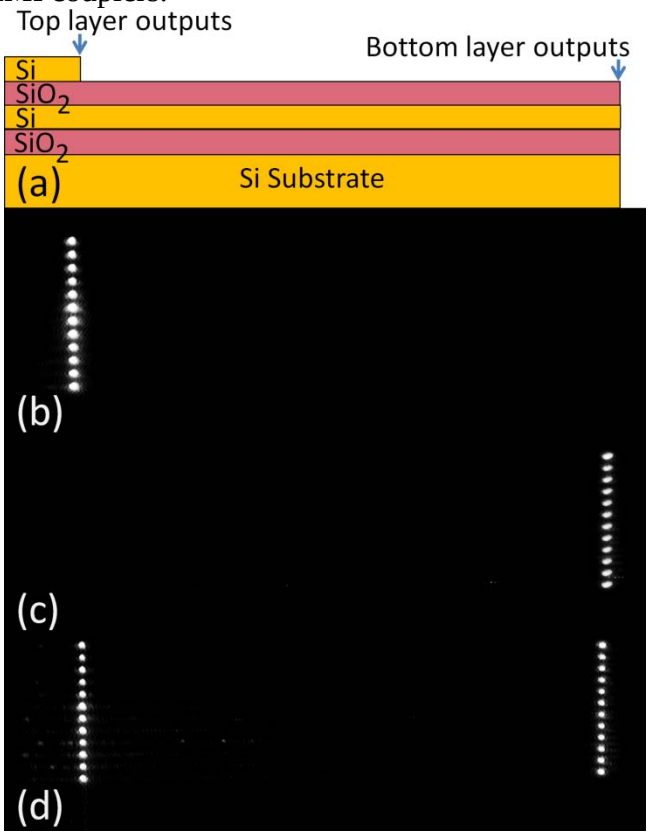

Figure 2-6: (a) Schematic of separated outputs for the top and bottom layers, (b) IR top-down image of the double-layer MMI coupler with top layer excitation, (c) IR top-down image of the double-layer MMI coupler with bottom layer excitation, (d) IR top-down image of the double-layer MMI coupler with simultaneous excitation to both layers.

We characterize the MMI couplers on both layers by fiber scanning as described in [11]. The chip is cleaved to make measurable facets via fiber for both the top and bottom layers. A single-mode lensed fiber (SMF) is used to scan each output channel to determine the output intensity of each channel and evaluate the performance of the MMI couplers on both layers. The uniformity of an MMI coupler is defined as $10\log(I_{max}/I_{min})$, where I_{max} and I_{min} are the maximum and minimum intensities of the MMI output

channels. The excess loss of an MMI coupler, which excludes the fiber-to-waveguide coupling loss and the waveguide propagation loss, is defined as $-\log[(\sum I_m)/I_{in}]$, where I_m is the intensity of the m^{th} output channel, and I_{in} is the output intensity of a reference waveguide on the same chip with the same cross section dimensions as the MMI access waveguides. Using FIMMPROP's fully vectorial eigenmode decomposition-based complex Film Mode Matching (FMM) solver (with 60 one-dimensional (1D) modes), we calculate the variations of the MMI excess loss and uniformity for both TE and TM polarizations [Figure 2-7]. Polarization independent operation is expected for a bandwidth larger than 30nm.

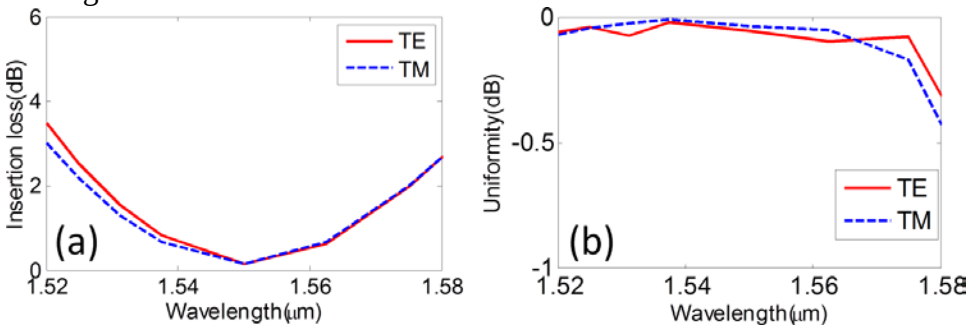

Figure 2-7: Simulated MMI (a) excess loss and (b) uniformity as functions of wavelength for TE and TM polarizations.

The top layer MMI coupler has an excess loss of 0.48 dB and a uniformity within 1.1 dB, while the bottom layer MMI coupler has an excess loss of 2.9 dB and a uniformity within 1.7 dB. Since the input waveguide is multimode, the excitation of TE_{0n} and TE_{mn} (m and n are the horizontal and vertical orders of the mode, m, n>0) modes depends on the input field launching condition, and consequently contributes to the excess loss and output non-uniformity. In our case, the input lensed fiber mode size ($1/e^2$) is 2.5 μm x 2.5 μm, and the input waveguide TE_{00} mode size is 2.2 μm x 1.1 μm (1.6 μm x 1.1 μm) for the bottom (top) layer. With optimized input coupling conditions, input

power is mostly coupled to the TE_{00} mode. The MMI performance is most efficient for the TE_{00} mode due to it having the highest effective modal index [11]. Under the excitation of the TE_{00} mode of the input waveguide, TE_{m0} modes will be excited, but TE_{0n} modes will not be excited inside the multimode waveguide region [Figure 2-1(a)]. By comparing the measured MMI performance metrics of both layers to 1xN MMIs fabricated on a 230 nm thick silicon nanomembrane (vertically single mode) [11], we confirm that the higher-order modes (inside the access waveguides) are suppressed with the optimized input coupling condition where most energy is coupled to the TE_{00} mode. We also find that bottom layer silicon membrane has larger thickness variations than the top layer silicon membrane, which contributes to the differences in device performance for each layer.

SUMMARY

In summary, we present vertically integrated, two-layer, low loss, crystalline silicon membranes. We developed a DRIE recipe for fabrication of self-aligned waveguiding structures on double-bounded SOI substrates. The fabricated double-layer MMI couplers show low excess loss [0.48 dB (top) and 2.9 dB (bottom)] and uniform outputs [within 1.1 dB (top) and 1.7 dB (bottom) power fluctuation] and can be used for 1-to-many fanouts on different layers in 3D silicon PICs. This approach is a potential solution to the limited silicon real estate problem via vertical integration of integrated photonic devices, such as optical phased arrays (OPAs) [16] and intra- and inter-chip guided wave optical interconnects [17, 18], which require accurate alignment between vertically integrated photonic devices.

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Chapter 3: Double-layer Photonic Devices Based on Transfer Printing of Silicon Nanomembrane

INTRODUCTION TO TRANSFER PRINTING PROCESS

In chapter 2, we present a method of fabricating self-aligned waveguiding structures on double-bonded SOI wafers through direct patterning and etching. This method, although delivers promising results for on-chip multi-layer silicon PICs, has several limitations that require further investigations. One issue is that the waveguides described in chapter 2 are multi-mode waveguides. To fully take the advantages of silicon photonics in on-chip optical interconnects, single-mode waveguides are usually preferred because they enable integration of higher density. As mentioned in chapter 1, single-mode silicon waveguides are fabricated on a silicon layer of with a thickness of only ~200 nm. This thin silicon layer can be viewed as a nanomembrane. Because of the limitation of processing tools, double-bonded SOI wafers with ~200 nm thick silicon device layers are not currently available from wafer manufacturers. To data, SOI wafers with ~200 nm thick silicon device layers are fabricated using the Smart CutTM technology from SOITEC. This is the most reliable source of silicon nanomembranes for pioneer research in electronics and photonics. Moreover, direct patterning and etching into double-bonded SOI wafers limits the devices on separated layers to be the same, which significantly limits the design flexibility. In this chapter, we demonstrate a novel 3D integration scheme using transfer printing of silicon nanomembranes.

Transfer printing based assembly techniques represents a potential transformational approach for micro/nanofabrication with far ranging fields of use [1, 2]. Transfer printing pre-fabricated inks onto other substrates have been demonstrated for different applications, including flexible silicon ICs [3] and epidermal electronics [4]. Transferrable silicon nanomembranes are prepared by isotropic wet etching of the BOX

layers of SOI wafers to release the silicon device layer from the silicon handle [5-7]. This approach serves as a promising solution to build a platform of multi-layer silicon nanomembranes for optical interconnects application. Considering the length of the waveguides in optical interconnects, it is very important to transfer print defect-free silicon nanomembranes with millimeter, or even centimeter dimensions, which has not been demonstrated in any aforementioned works. We developed a transfer printing process to transfer print silicon nanomembranes with dimensions of 8.05mm x 2.05 mm. The principle of the deterministic transfer printing in our process is described in [2].

TRANSFERRABLE SILICON NANOMEMBRANE FABRICATION

The fabrication process for large-area, transferrable silicon nanomembranes is illustrated in Figure 3-1. A SOI chip with a silicon device layer of 230 nm and a BOX layer of 1μm is used as the source for silicon nanomembranes. Note that the original silicon device layer thickness is 340 nm, we thermally oxidized the SOI chip and removed the oxide layer using HF wet etching, leaving a silicon device layer of 230 nm (Figure 3-1(a)). The silicon nanomembrane, whose dimensions are 8.05 mm x 2.05 mm, is defined using optical lithography and SF_6 based RIE. Several rows of holes are also defined on the silicon nanomembranes to let HF etch the BOX layer beneath the silicon nanomembranes in the silicon nanomembrane release step, as shown in Figure 3-1(b). Next, the SOI chip with defined silicon nanomembranes is wet etched in HF for 55 seconds to partially undercut the BOX layer, this step creates rooms for photoresist anchor to support silicon nanomembranes in the silicon nanomembrane release step (Figure 3-1(c)). Photoresist (AZ 5214) is then spun onto the SOI chip, flood exposed with optical lithography, and developed, leaving the photoresist in the undercut beneath the silicon nanomembranes, as shown in Figure 3-1(d). The photoresist left serves as anchors

to support silicon nanomembranes. The SOI chip is then wet etched in HF for 19 hours to fully remove the BOX layer and release the defined silicon nanomembranes. Finally, the fabricated silicon nanomembranes are retrieved with PDMS stamp (Figure 3-1(e)).

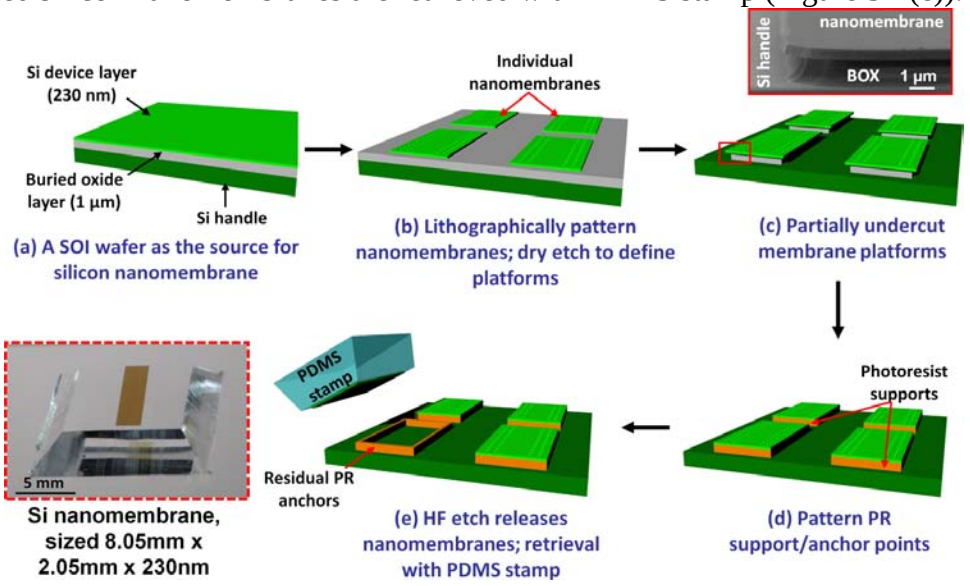


Figure 3-1: The process flow to fabricate large-area, transferrable silicon nanomembranes.

SINGLE-LAYER MMI DESIGN AND FABRICATION

As a proof of concept, we designed MMI couplers on silicon nanomembranes for double-layer device demonstration. A schematic of the MMI coupler is previously shown in Figure 2-1(a). MMI devices operate based on the phenomenon of self-imaging in multimode waveguides whereby an input field profile is reproduced in single or multiple images at periodic intervals along the propagation direction of the guide [8]. We choose the width of the MMI, W_{MMI}=60 µm, and the length of the MMI is given by $L_{MMI} = (n_{eff} W_{MMI}^2)/(\lambda_0 N)$, which is L_{MMI}=553.4 µm. n_{eff}=2.86 is the effective refractive index of the TE fundamental mode in the multi-mode waveguide, λ_0=1.55 µm is the operating wavelength, and N=12 is number of outputs. The input and output access waveguides' width, W_w is chosen to be 2.6 µm. At this width, the modal phase errors are

greatly reduced, thereby enhancing the output uniformity of our MMI coupler [9]. We performed a simulation of our MMI coupler using Rsoft's BeamPROP software based on beam propagation method. As can be seen from Figure 3-2, our simulation shows good output uniformity when using TE polarized light at 1550 nm.

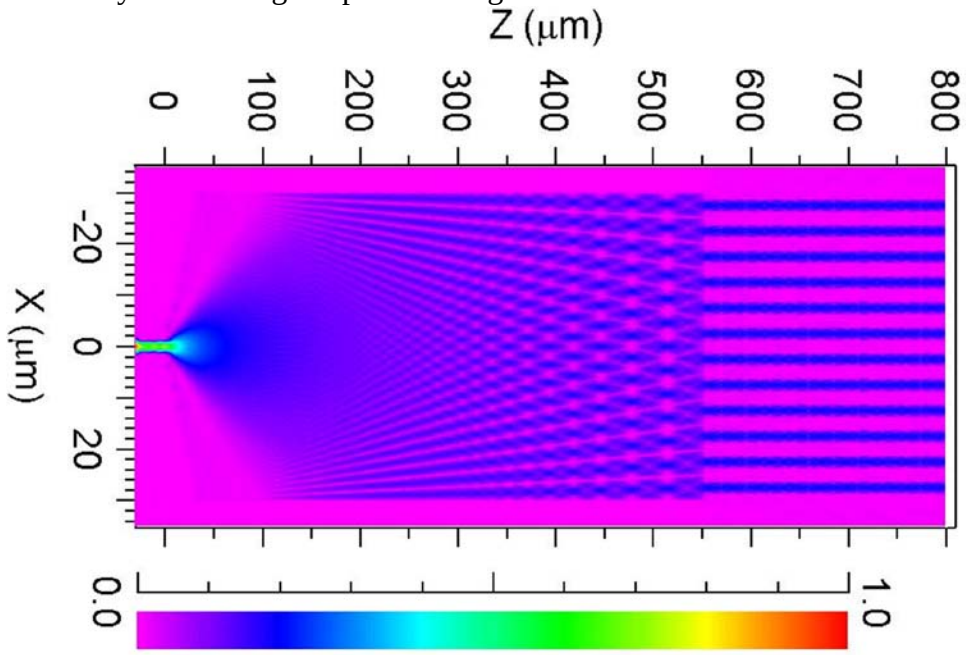


Figure 3-2: MMI performance simulated by BeamPROP.

The fabrication process of MMI couplers on SOI wafers is illustrated in Figure 3-3 [10]. SOI wafers with silicon device layer of 250 nm and BOX layer of 3 μm are thermally oxidized to consume a silicon thickness of 20 nm and form ~44 nm thick silicon oxide. This silicon oxide serves as the hard mask for silicon etching. Device patterning is done with EBL with positive EB resist, ZEP 520A. In order to reduce the writing time of EBL, instead of writing trenches to define a waveguide between two trenches, we directly write the device pattern with EBL, and using a nickel lift-off process to reverse the pattern. Nickel is deposited using electron beam evaporation and lifted-off by Remover PG from MicroChem. Device pattern on 20 nm thick nickel layer

is transferred to silicon oxide using CHF3/O2 based RIE, and then transferred to silicon device layer using HBr/Cl2 based RIE. Finally, the nickel layer is removed in piranha solution, and a 1µm thick silicon oxide layer is deposited onto the fabricated devices using PECVD as top cladding.

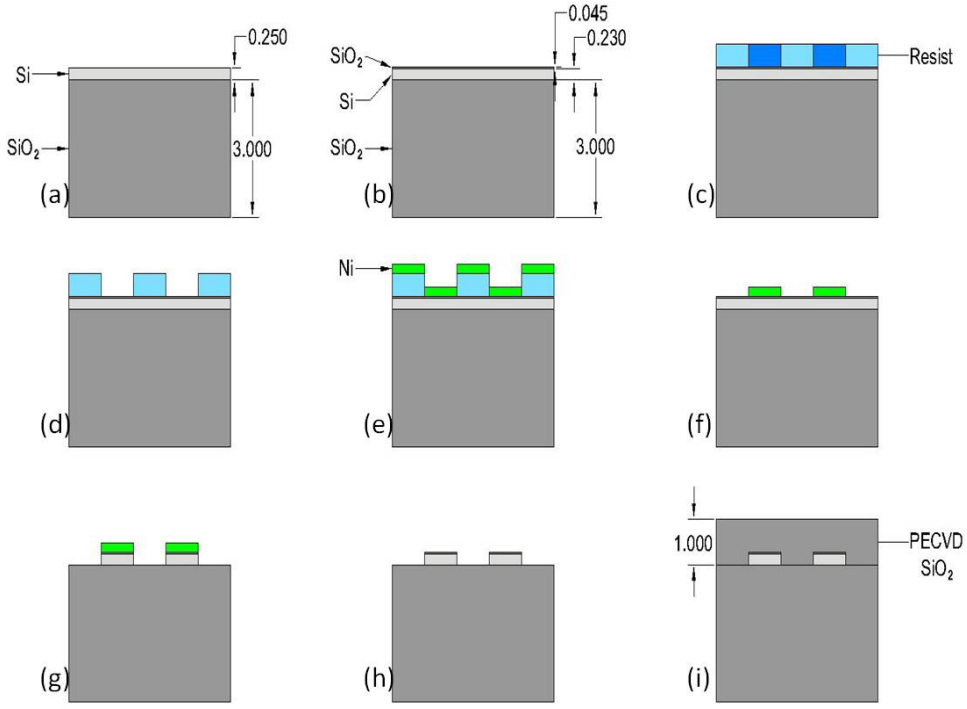


Figure 3-3: The process flow to fabricate single-layer MMI devices. (a) SOI wafer with 250 nm device layer and 3 µm BOX layer, (b) thermal oxidation to create a silicon oxide layer, (c) EBL, (d) resist development, (e) nickel deposition, (f) nickel lift-off, (g) silicon oxide etching, (h) silicon etching, (i) top cladding deposition.

DOUBLE-LAYER MMI FABRICATION AND CHARACTERIZATION

Figure 3-4(a) provides a schematic demonstration of the assembly process for double-layer silicon nanomembrane device platform through transfer printing and patterning steps. The device fabrication started with commercially available SOI from SOITEC with 3 µm buried oxide layer (BOX) and 250 nm silicon device layer. The

design and fabrication of MMI coupler on the bottom layer using electron beam lithography (EBL) and reactive-ion-etching (RIE) was described in the above section. After etching of the silicon device layer, a silicon dioxide layer of 1.5 μm (instead of above-mentioned 1 μm) was deposited using plasma-enhanced chemical vapor deposition (PECVD) as the interlayer dielectric between the bottom and top layer. Next, a thin layer (~500 nm) of SU8 epoxy adhesive was spin-cast onto the silicon dioxide surface. Partial curing of the adhesive layer via heating and UV flood exposure provided a flat, firm surface for mounting additional nanomembrane as top layer.

Silicon nanomembrane derived from a SOI wafer and measuring 2.05 mm x 8.05 mm x 230 nm were released from the hosts by etching in concentrated (49%) HF and retrieved by a bulk piece of PDMS mounted to a rigid glass backing. Figure 3-4(b) shows a single silicon nanomembrane on the surface of the stamp after retrieval. The inked PDMS was brought into contact with the adhesive-bearing material stack using a custom alignment system with an integrated heating platform. While in contact, the stamp/nanomembrane/substrate system was heated to ~70°C for 10 minutes to fully cure the adhesive. After curing, the stamp is slowly (~500 μm/s) retracted from the surface, transferring the aligned silicon nanomembrae to the material stack as the top device layer. Figure 3-4(c) shows the silicon nanomembrane printed onto the multilayer stack. A silicon dioxide layer of 40 nm was deposited using electron beam evaporation as the hard mask for silicon nanomembrane etching. The MMI coupler on the top silicon nanomembrane layer was patterned using EBL and negative EB resist, NEB31A3. The MMI pattern was transferred into deposited silicon dioxide layer using CHF3/O2 based RIE, and then transferred into silicon nanomembrane layer using HBr/Cl2 based RIE. The resist is finally removed with acetone.

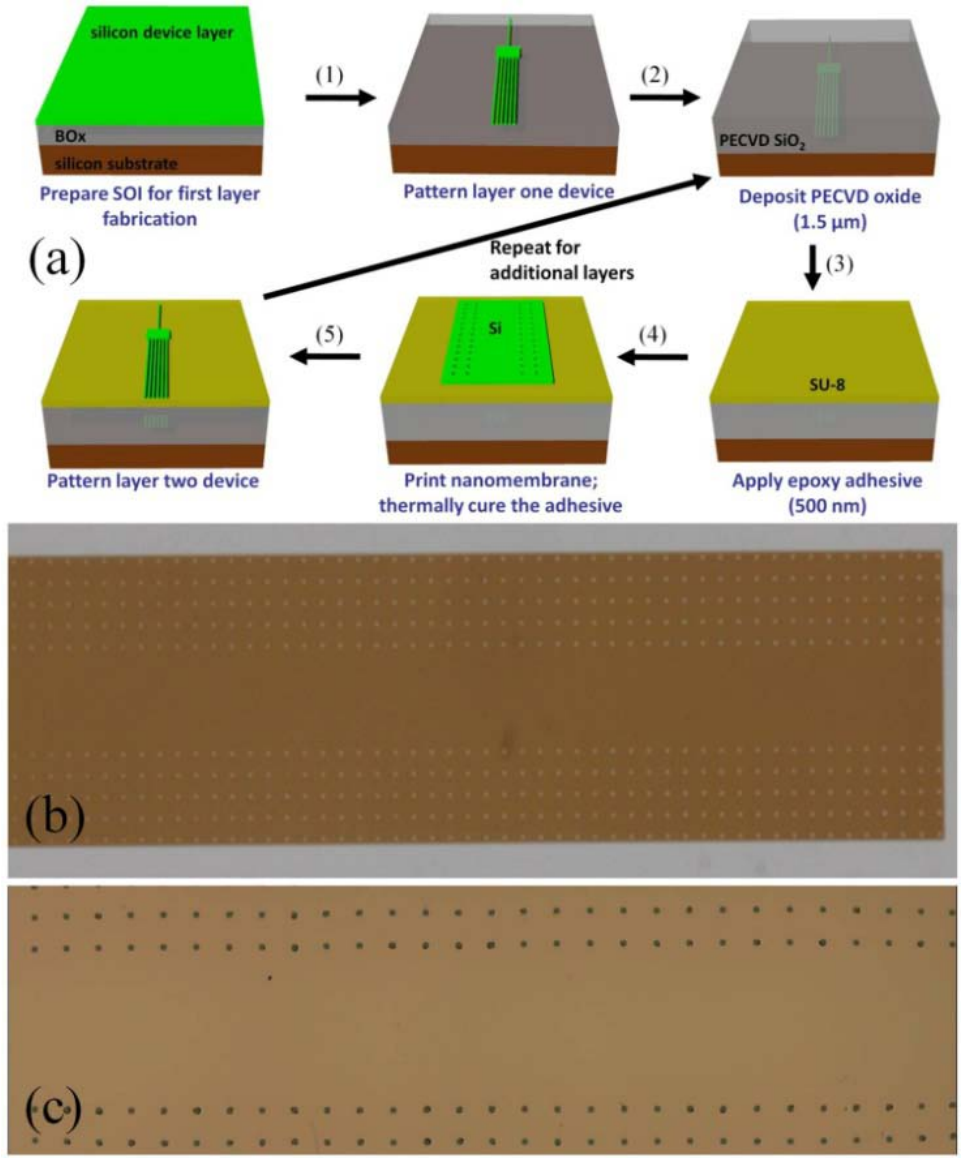


Figure 3-4: (a) Schematic process flow for assembling double-layer device on silicon nanomembrane, (1) single-layer MMI fabrication, (2) silicon oxide deposition, (3) SU-8 spin-on, (4) silicon nanomembrane transfer printing, (5) single-layer MMI fabrication, (b) Silicon nanomembrane on the stamp after retrival, (c) Silicon nanomembrane on the multilayer stack.

An optical microscope microscope image of the fabricated double-layer MMI is shown in Figure 3-5(a). A SEM image of the fabricated MMI on the transfer printed

silicon nanomembrane is shown in Figure 3-5(b). A cross-sectional SEM image of one double-layer output waveguide is shown in Figure 3-5(c). The corresponding positions of the parts in Figure 3-5(b) and 3-5(c) is labeled in Figure 3-5(a).

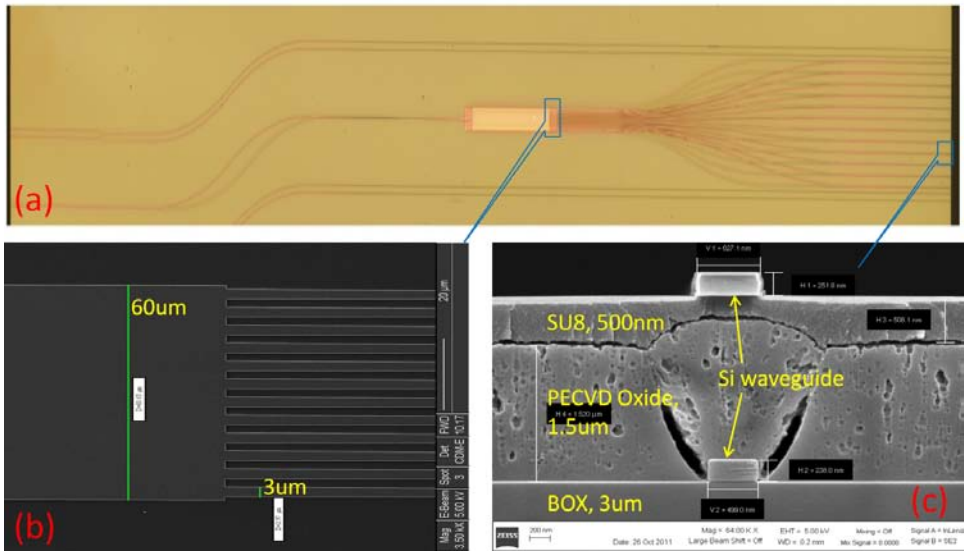


Figure 3-5: (a) An optical microscope image of the fabricated double-layer MMI, (b) A SEM image of the fabricated MMI on transfer printed silicon nanomembrane, (c) A cross-sectional SEM image of a double-layer output access waveguide.

In order to characterize the performance of the fabricated double-layer MMI, an automated aligner system was used to couple TE polarized light at 1550 nm from a PMF with a 2.5 μm output mode diameter into the waveguide inputs. The waveguide facet was prepared using cleaving. An IR CCD camera connected to a variable objective lens captured the top-down near field images of the output waveguides' facets. These facets are defined with RIE. A fanout design was used to increase the separation of each output waveguide to 30 μm for resolve the 12 output intensities for near field imaging. In order to separate the outputs in the bottom layer from those in the top layer, we etched the output waveguides of the top layer to terminate them before where the bottom layer

waveguides end as shown in Figure 3-6(a). Figure 3-6(b) shows a top-down IR image of simultaneous excitation of MMI couplers on both layers.

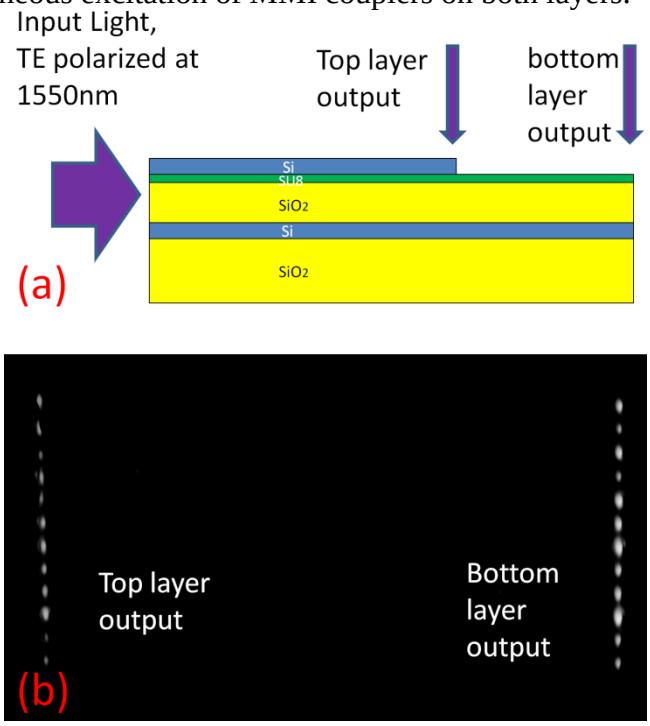
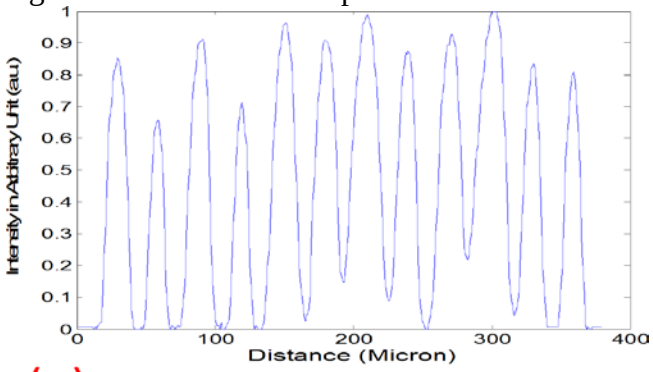


Figure 3-6: (a) A schematic showing separated outputs of bottom and top layers, (b) An top-down IR image of the two 1x12 MMI couplers with simultaneous excitation.

One important issue about the above-mentioned testing setup is that the waveguide facets prepared using cleaving may not be exactly at the cleaving facet. This is because that the SU-8 does not have a crystal orientation and the mechanical strength of the Si/SU8 interface is not strong enough. As a result, the cleaved waveguide facets can be away from the cleaving facet by a few micron, which make butt-coupling to waveguides nearly impossible, and thus disable the fiber scanning method to measure the intensities from individual output waveguides. An alternative approach to characterize the uniformity of MMI output is to analyze the top-down IR image. By analyzing the intensities of individual light spots in top-down IR image, as shown in Figure 3-6(b), we

got the uniformity of MMIs on both layers, as shown in Figure 3-7. The uniformity of an MMI coupler is defined as $10\log(I_{max}/I_{min})$, where I_{max} and I_{min} are the maximum and minimum intensities of the MMI output channels. The uniformity of the MMI on bottom layer is calculated to be 1.8dB, and that of the MMI on top layer is calculated to be 3.7dB. The discrepancy between uniformities of MMIs on different layers is due to the difference in the fabrication processes to fabricate MMIs on different layers. We believe the performance of MMI on transfer printed nanomembrane can be improved by optimizing the related fabrication process.



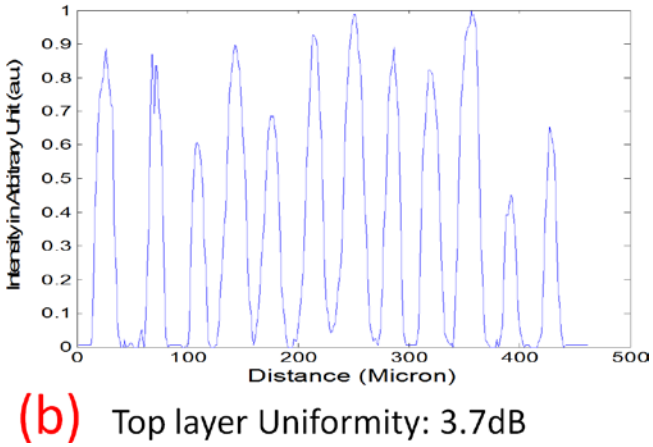


Figure 3-7: (a) The output uniformity of the bottom layer MMI coupler, (b) The output uniformity of the top layer MMI coupler.

SUMMARY

In summary, we present a novel vertical integration scheme of large photonic components on multi layers of low loss crystalline silicon nanomembranes by using transfer printing techniques. We developed the patterning and printing process for fabricating double-layer photonic devices and this process can be expanded to large numbers of stacked nanomembrane based photonic devices by repeating the patterning and printing steps. This scheme is a potential solution to the limited silicon real estate for vertical integration of integrated photonic devices, and also serves as platform for novel forms of integrated optical devices.

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Chapter 4: On-chip Intra- and Inter-layer Grating Couplers for 3D Integration of Silicon Photonics

INTRODUCTION TO GRATING COUPLER AND SUBWAVELENGTH NANOSTRUCTURE

In chapter 3, one issue about devices on silicon nanomembranes is raised, that is how to efficiently couple light into waveguides with submicron dimensions. Even the waveguide facets are perfectly defined, the mode mismatching between single-mode silicon waveguides and single mode fibers, which have core diameters of 9 μm will lead the huge coupling loss. In the previous chapters, we tapered the single-mode silicon waveguides to 2.5 μm wide at the waveguide facets, and used lensed fiber with a mode diameter of 2.5 μm to do butt-coupling between waveguides and lensed fibers, which still lead to ~10 dB coupling loss per waveguide/fiber interface. Efficient butt-coupling between waveguides and SMFs can be done using inverse taper [1]. The highest coupling efficiency demonstrated so far is ~0.5 dB for TE polarization [2]. In order to achieve such low coupling loss, the inverse taper tip has to be sufficiently narrow (e. g. 30nm) to stimulate a delocalized mode. This critical lithography requirement lowers the overall yield of photonic devices. Furthermore, inverse tapers will not provide mode sizes comparable to SMF mode sizes [3, 4], thus customized lensed fibers are still required. In order to let fiber access to inverse taper, precise dicing and polishing are usually required [4], which limits the applications of inverse taper in wafer scale testing. An alternative solution for achieving high fiber-to-chip coupling efficiencies is the use of a grating coupler [5-7]. The grating coupler diffracts and redirects in-plane light into out-of-plane light propagating in different directions. The grating diffraction is governed by the phase matching condition, which is given by $k_0 n_{eff} = k_0 n_c \sin\theta + q\frac{2\pi}{\Lambda}$, where $k_0 = 2\pi/\lambda$, n_c is the refractive index of the cladding material, θ is the angle of the output light from surface-normal, n_{eff} is the average effective refractive index for the optical mode in the

grating, and q is an integer representing the diffraction order, which is 1 within the discussion of this chapter, and Λ is the period of the grating.

In order to enhance the coupling efficiency, additional steps, including shallow etching [5], epitaxial silicon overlay [6], bottom reflector [5], and RIE lag effect [7], have been introduced to the fabrication of grating couplers on SOI platform. These additional steps will keep increasing the complexity of fabrication process of silicon PICs, especially when multi-layered silicon PICs are to be fabricated. Ideally, grating couplers would be patterned and through-etched in the same step as part of the PICs. However, considering the high index contrast between silicon and cladding materials (air/silicon oxide), the Fresnel reflection is prohibitively high at the silicon/cladding interfaces. One idea comes to mind is to use material with higher index to fill the through-etched trenches. However, such material does not naturally exist in CMOS process. One possible solution is to use artificial materials with variable refractive indices. Using subwavelength nanostructure as a low-index material in grating couplers, which was first proposed in 2009 [8], delivers several promising results for on-chip fiber-to-chip application, for both TE and TM polarizations [9-11]. In the following sections, we discuss the design, fabrication and testing of subwavelength nanostructure based intra- and inter-layer grating couplers on multi-layer silicon nanomembranes.

ENGINEERING THE REFRACTIVE INDEX OF SUBWAVELENGTH NANOSTRUCTURE

One main advantage of using subwavelength nanostructure in grating coupler is that its refractive index can be engineered to accommodate different grating designs. In this chapter, 1D stratified structure, which comprising silicon and periodically through-etched holes interleaved at the subwavelength scale, is chosen as the low-index material in grating coupler designs [11]. According to effective medium theory (EMT) [12], a

composite medium comprising two different interleaved at the subwavelength scale can be approximated as a homogenous medium with a refractive index between these two materials. For TE polarization, the refractive index of the subwavelength nanostructure can be calculated using [13]:

$$\frac{\sqrt{n_{si}^2 - n_{TE}^2}}{n_{si}^2}\tan\left(\frac{\pi\sqrt{n_{si}^2 - n_{TE}^2}(\Lambda_{sub} - W_{sub})}{\lambda}\right) = -\frac{\sqrt{n_{hole}^2 - n_{TE}^2}}{n_{hole}^2}\tan\left(\frac{\pi\sqrt{n_{hole}^2 - n_{TE}^2}W_{sub}}{\lambda}\right) \quad (1)$$

Where n_{TE} is the refractive index of SWN for TE polarization. n_{si} and n_{hole} are the refractive indices of the silicon and the material in the holes, respectively. Λ_{sub} is the period of the subwavelength nanostructure, and W_{sub} is the width of the rectangular through-etched holes.

As Equation (1) does not have an explicit analytical solution, second-order polynominal expansion is used to approximate the tangent function, lead to the equation we used in engineering the refractive of subwavelength nanostructure [14]:

$$n_{TE}^2 = n_{TE}^0\left(1 + \frac{\pi^2}{3}\left(\frac{n_{effTE}\Lambda_{sub}}{\lambda}\right)^2 f_{sub}^2(1 - f_{sub})^2(n_{hole}^2 - n_{si}^2)^2\left(\frac{n_{TM}^0}{n_{effTE}}\right)^2\left(\frac{n_{TE}^0}{n_{hole}n_{si}}\right)^4\right)^{1/2} \quad (2)$$

Where n_{TE}^0 and n_{TM}^0 is the refractive index of the SWN using zero-order polynominal expansion in TE and TM polarization, respectively, $f_{sub} = W_{sub}/\Lambda_{sub}$, and n_{effTE} is the effective refractive index of the slab waveguide mode in silicon nanomembrane in TE polarization. Equation (2) shows that when Λ_{sub} is fixed, the refractive index of subwavelength nanostructure will increase with the decrease of f_{sub}, thus the decrease of W_{sub}.

DESIGN OF INTRA-LAYER GRATING COUPLERS

Schematics of our intra-layer grating couplers are shown in Figure 4-1. Considering a platform consisting of two vertically integrated silicon nanomembranes, which can be realized by transfer printing or bonding one silicon nanomembrane onto a SOI wafer, we designed two different intra-layer grating couplers, for fiber-to-chip coupling to silicon nanomembrane on bottom layer and top layer, respectively, as shown in Figure 4-1(a) and Figure 4-1(b), respectively. A top-view of the schematic of subwavelength nanostructure based grating is shown in Figure 4-1(c). Silicon and subwavelength nanostructures are periodically placed along the direction of light propagation, and the subwavelength nanostructure is defined by periodically interleaved silicon and etched holes along the direction perpendicular to light propagation.

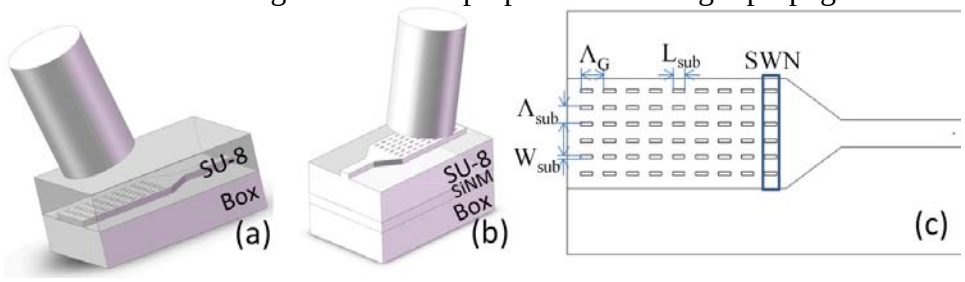

Figure 4-1: Schematics of (a) Fiber-to-bottom-layer intra-layer grating coupler, (b) Fiber-to-top-layer intra-layer grating coupler, (c) Subwavelength nanostructure based grating coupler. (SiNM denotes silicon nanomembrane, SWN denotes subwavelength nanostructure)

The intra-layer grating to bottom layer has a silicon oxide bottom cladding (BOX layer of a SOI wafer) and a SU-8 top cladding. The intra-layer grating to top layer has a SU-8 bottom cladding and air top cladding. We used a 2D simulation package CAMFR based on eigenmode expansion to perform an exhaustive parameter sweep of their grating period (Λ_G) and subwavelength nanostructure's refractive index (n_{sub}) combinations. Grating duty cycle was fixed to be 50%, which corresponds to $L_{sub}=\Lambda_G/2$. Input light was

assumed to be TE polarized. The grating coupling efficiencies are also dependent on the thicknesses of bottom cladding layers [15]. However, these thicknesses were limited by the SOI wafers available and the processes to form the multi-layer structure.

We found that the maximum power-up efficiency is 26% with Λ_G=735 nm and n_{sub}=2.15 at a power-upward angle of 14° from normal incidence for the intra-layer grating coupler to bottom layer, when the bottom layer thickness is 3 μm, and the maximum power-upward efficiency is 59% with Λ_G=690 nm and n_{sub}=2.45 at a power-upward angle of 10° from normal incidence, when the bottom layer thickness is 3.7 μm. Figure 4-2(a) and Figure 4-2(b) show bottom and top grating coupler model in the simulations, respectively. Light are coupled out from the waveguides through the grating couplers. The electric field distributions calculated by CAMFR with the optimized parameters are shown in Figure 4-2(a) and Figure 4-2(b). In order to engineer the subwavelength nanostructure's refractive index to be 2.15 (2.45), we choose Λ_{sub}=390 nm, and the corresponding W_{sub} is calculated to be 202 (80) nm. We used 23 (25) grating periods and 32 (26) subwavelength periods in our grating coupler, which correspond to a grating coupler size of 17 μm x 13 (10) μm, to match the mode diameter of SMF.

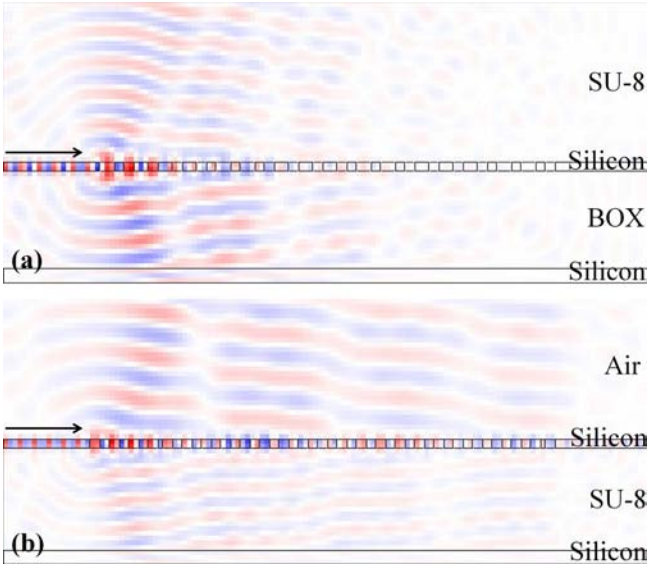

Figure 4-2: Calculated electric field distribution using CAMFR with optimized parameters for (a) Fiber-to-bottom-layer grating coupler, (b) Fiber-to-top-layer grating coupler.

DESIGN OF INTER-LAYER GRATING COUPLERS

Multi-layer silicon photonic platforms have been demonstrated with film deposition approaches, including hydrogenated amorphous silicon, polycrystalline silicon and silicon nitride [16-18]. The pros and cons of these materials have been discussed in chapter 1. Another approach is to use direct bonding to build multi-layer PICs [19]. This method requires high bonding temperature, which is not compatible with CMOS back-end process. Despite their potentials to build multi-layer silicon PICs, an efficient coupling mechanism between layers is necessary to realize signal transmission through the PIC. One promising solution is a directional coupler type vertical coupler. This structure requires keeping the distance between two layers around 200 nm [20], which is usually not enough to provide optical isolation between layers. Although the results in [19] indicate that directional coupler type vertical coupling is possible for distance between layers around 1μm, it is not clear if this approach can work for inter-layer

coupling between silicon PICs, in which optical modes are tightly confined. It is necessary to develop a coupling mechanism when the distance between layers is large. One possible approach is to use grating couplers for inter-layer coupling, as demonstrated with amorphous silicon layers [21].

Various grating couplers have achieved coupling between photonic layers [22-24]. However, these are only suitable for inter-chip applications. To date, on-chip inter-layer grating coupling was accomplished with amorphous silicon layers, but single crystalline silicon layers are preferable as stated in chapter 1. In this section, we design the inter-layer grating coupler based on the structure in which a silicon nanomembrane is transferred or bonded onto a single-layer silicon PIC fabricated on a SOI wafer as an additional layer for photonic device fabrication. The realization of this structure will be discussed in the next section.

Figure 4-3 shows a 3D schematic of the inter-layer grating coupler integrated with fiber-to-chip intra-layer grating couplers. Light is coupled from a PMF with a core diameter of 9 μm to an area-matched linearly tapered waveguide follow by a 2.5 μm wide waveguide on the bottom layer through grating 1, and then coupled to a 2.5 μm wide waveguide on the top layer though inter-layer grating coupler, which consists of grating 2 and grating 3. The light is then coupled out to a SMF with a core diameter of 9 μm through grating 4. The grating regions are connected to 2.5 μm wide waveguides using 500 μm long linear tapers. The two silicon nanomembranes on different layers are 0.25 μm thick with refractive indices of 3.47. The BOX layer has a thickness of 3 μm, and a refractive index of 1.45. The gratings on both layers are formed by periodically patterning parts of silicon layer into subwavelength nanostructures, whose refractive indices can be engineered to accommodate grating coupler design. Such nanostructures provide high coupling efficiency with large optical bandwidth while providing anti-

reflection mechanism through destructive interference [11]. Subwavelength nanostructure based gratings can be patterned and etched in the same step with the silicon waveguide layer, and thus simplify the fabrication process.

The design of subwavelength nanostructure follows the method described in previous section. Figure 4-3 shows a schematic of 1D stratified subwavelength nanostructure used in our grating couplers. Silicon and etched rectangular holes are periodically laminated to form the subwavelength nanostructrure. Λ_{sub} is the period of subwavelength nanostructure, W_{sub} is the width of the rectangular etched hole, and Lsub is the length of the rectangular etched hole. The refractive index of the subwavelength nanostucture (n_{sub}) is a function of Λ_{sub}, W_{sub}, operating wavelength (λ), and the refractive index of the material in the etched holes (n_{hole}) [14], and can be engineered by tuning W_{sub} with a fixed Λ_{sub}. The gratings based on subwavelength nanostructure are treated as conventional grating couplers in the inter-layer grating coupler design described below.

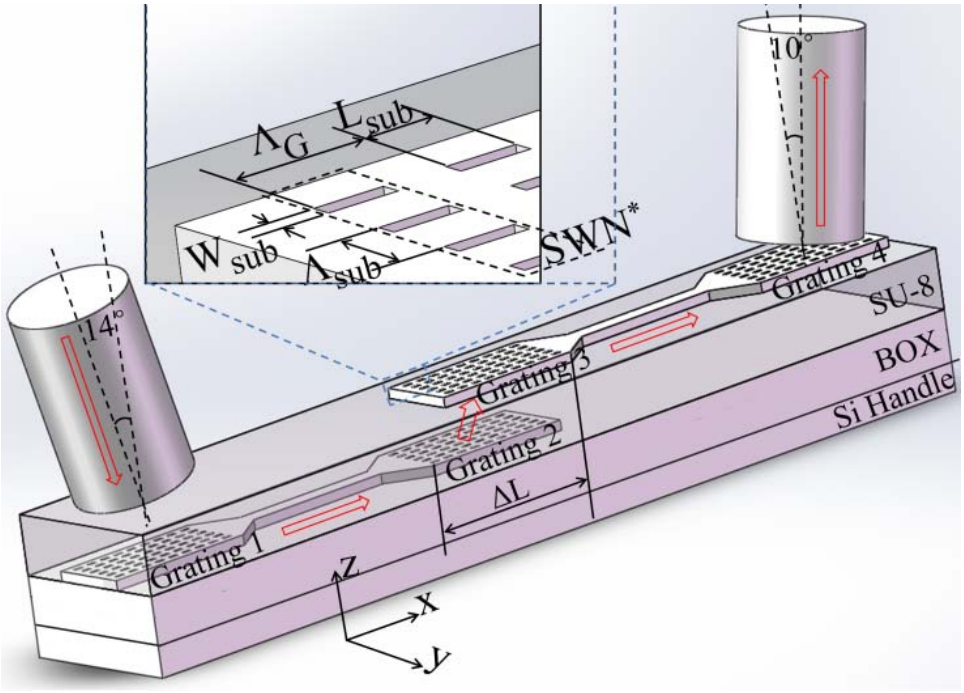

Figure 4-3: A 3D schematic of the intra- and inter-layer grating couplers (*SWN denoted subwavelength nanostructure).

The inter-layer grating coupler consists of grating 2 and grating 3. We used 25 periods and 50% grating duty cycle ($L_{sub}=\Lambda_G/2$) for both grating 2 and grating 3. Grating period (Λ_G), grating 2's subwavelength nanostructure's refractive index (n_{sub1}), grating 3's subwavelength nanostructure's refractive index (n_{sub2}), SU-8 layer thickness (t_{SU-8}) and effective length (ΔL), which is defined as the distance between the start of grating 2 and the end of grating 3, were optimized by 2D FDTD simulations. The input light is assumed to be TE polarized at 1550 nm operating wavelength. We found that the maximum coupling efficiency of the inter-layer grating coupler is 21% with Λ_G=820 nm for both grating 2 and grating 3, n_{sub1}=2.5, n_{sub2}=2.55, t_{SU-8}=3.7 μm and ΔL=12.0 μm. We used Λ_{sub}=390 nm for the subwavelength nanostructures of both grating 2 and grating 3. W_{sub} of grating 2 was calculated to be 141 nm with n_{hole}=1.575 and n_{sub}=2.5. W_{sub} of grating 3 was calculated to be 70 nm with n_{hole}=1 and n_{sub}=2.55. Here we assumed that

the etched holes of grating 2 (on the bottom layer) are filled with SU-8, so n_{hole} equals to the refractive index of SU-8 (n_{SU-8}=1.575), and the etched holes of grating 3 (on the top layer) are filled with air, so n_{hole} equals to the refractive index of air (n_{air}=1).

Figure 4-4 shows the electric field distribution calculated by 2D FDTD simulations with the optimized structural parameters. Light is coupled from the waveguide on the bottom layer to the waveguide on the top layer through the inter-layer grating coupler. Different colors represent the intensity of the electric field. Note that the power upward emitting angle of grating 2 and the power downward emitting angle of grating 3 are both 22° in our design at 1550 nm operating wavelength.

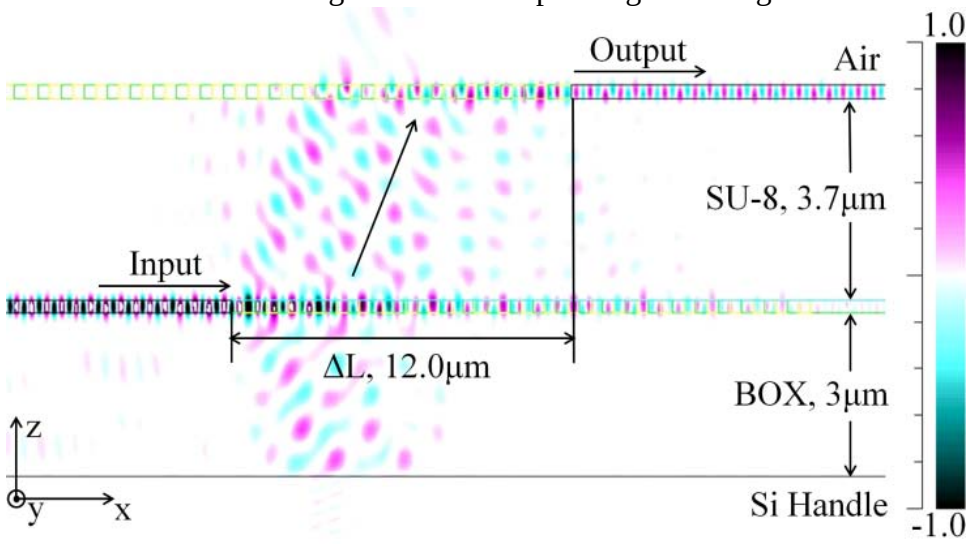

Figure 4-4: The electrical field distribution of the optimized inter-layer grating coupler calculated using 2D FDTD.

The design of grating 1 and grating 4 follows the method described in previous section. Grating 1 is 17 μm long and 13 μm wide, with a Λ_G of 735 nm and a grating duty cycle of 50%. It has a Λ_{sub} of 390 nm and a W_{sub} of 202 nm, which correspond to n_{sub} of 2.15. Grating 4 is 17 μm long and 10 μm wide, with a Λ_G of 690 nm and a grating duty cycle of 50%. It has a Λ_{sub} of 390 nm and a W_{sub} of 80nm, which correspond to n_{sub} of

2.45. The size of grating 4 was chosen to match the mode size of a SMF. The width of grating 1 was chosen to be larger than that of grating 4 to account for the field divergence induced by light propagating in the SU-8 layer on top of grating 1, as well as to increase the fiber-to-chip alignment tolerance. The parameters of grating 1, 2, 3 and 4 are summarized in Table 4-1. For grating 2 and grating 3, their lengths were given by aforementioned simulations. Grating 3 was designed to be wider than grating 2 to compensate for the field divergence as light propagates in the SU-8 layer, as well as to increase the alignment tolerance between two layers in y-direction (as defined in figure 4-3).

Table 4-1: The parameters of grating 1, 2, 3 and 4.

	Length (μm)	Width (μm)	# of grating period	Λ_G (nm)	# of subwavelength period	Duty cycle	Λ_{sub} (nm)	W_{sub} (nm)	n_{sub}
Grating 1	17	13	23	735	32	50%	390	202	2.15
Grating 2	20.5	10	25	820	26	50%	390	141	2.5
Grating 3	20.5	13	25	820	32	50%	390	70	2.55
Grating 4	17	10	25	690	26	50%	390	80	2.45

DEVICE FABRICATION

The transfer printing process presented in chapter 3 is a promising way to build multi-layer silicon PIC. However, the size of the transfer printed silicon nanomembrane is still limited in one direction. Ideally, the size of the silicon nanomembrane should be comparable to the die size. Wafer bonding is a well developed technique to build 3D structure in microelectronics and micro-electro-mechanical systems (MEMS). Adhesive bonding, which has been used in fabricating nanophotonic devices on silicon nanomembrane [25], serves as a good candidate for fabricating multi-layer silicon PICs.

In this section, we present a fabrication process utilizing SU-8 adhesive bonding to build on-chip, double-layer silicon nanomembranes. The fabrication process flow of the devices is illustrated in Figure 4-5. Gratings on the bottom layer were fabricated on an SOI chip (250 nm single crystalline silicon device layer and 3 μm BOX layer) using EBL with Zep520A positive e-beam resist and HBr/Cl2 based RIE. Note that in this process, the waveguides were defined by etching two trenches beside the waveguide, so that most of the silicon device layer remained after RIE. This SOI chip served as recipient substrate in adhesive bonding process. Another SOI chip was used as donor substrate in adhesive bonding process (Figure 4-5(a)). Both chips were cleaned with piranha solution and Buffered Oxide Etch (BOE) before bonding. A five minutes dehydrating bake at 150° were also applied to the chips to ensure high quality SU-8 layers in spinning-on. ~2 μm thick SU-8 layers were spun onto both the recipient and donor substrates using SU-8 2002 resist at 3000rpm, followed by a 2 minute pre-bake at 95°C to evaporate the solvent (Figure 4-5(b)). SU-8 has excellent self-planarization characteristics and low optical loss [26] at the optical communication wavelength range, which make it an ideal adhesive material in our fabrication process. Next, the two substrates were brought in close contact using a home-made chip bonder, which uniformly applied pressure, and kept in a 90°C oven to ensure sufficient reflow of SU-8 for trapped air bubble removal to give high quality bond (Figure 4-5(c)). After adhesive bonding, the silicon handle of the donor substrate was first polished down to ~100 μm thick, and then removed by SF6/C4F8/Ar based Deep Reactive Ion Etching (DRIE). The BOX layer of the donor substrate served as an etch-stop layer in the DRIE process, and also protected the device layer of the donor substrate before future process. After the silicon handle was removed, the SU-8 layer was exposed to ultraviolet (UV) irradiation through the donor substrate and post-baked for UV induced polymer crosslinking and hardening. The BOX layer of the donor

substrate was then removed by wet etching in 49% hydrofluoric acid (Figure 4-5(d)). This adhesive bonding process results in a SU-8 layer thickness of 3.7 μm. Finally, gratings were fabricated on the top layer using EBL and RIE (Figure 4-5(e)).

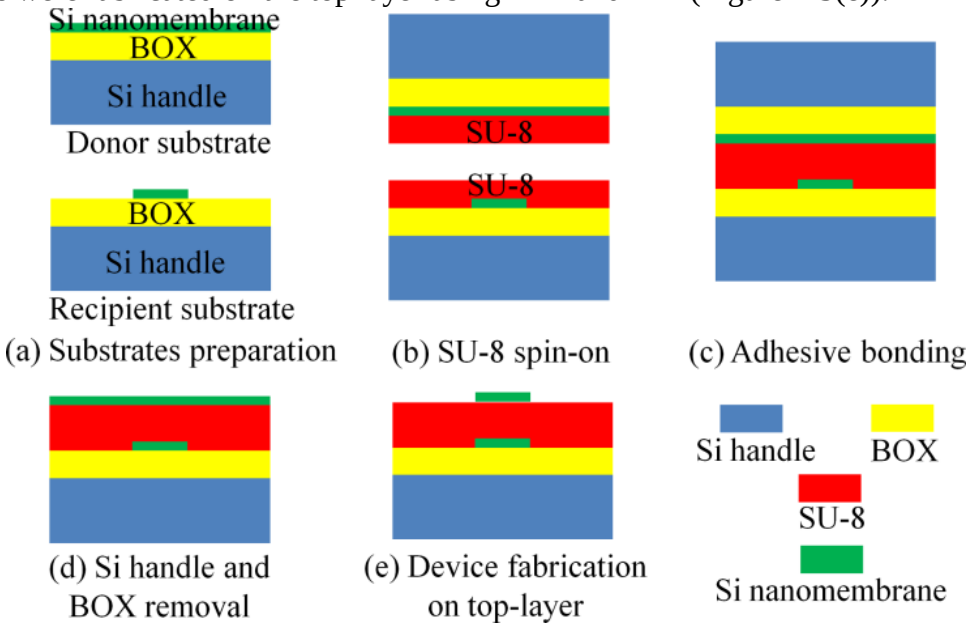

Figure 4-5: A schematic of the fabrication process flow, (a) substrates preparation, (b) spinning-on SU-8 onto substrates, (c) adhesive bonding, (d) si handle and BOX removal, (e) device fabrication on top-layer.

A cross-sectional SEM image of the bonded double-layer silicon nanomembranes is shown in Figure 4-6(a). A SEM image of a fabricated grating on the bottom layer before adhesive bonding is shown in Figure 4-6(b). Note that the rectangular etched holes on the bottom layer were filled with SU-8 during the bonding process, as shown in Figure 4-6(c). The alignment between gratings on top and bottom silicon nanomembranes within 100 nm accuracy was realized by electron beam scanning of gold alignmarks on the bottom silicon nanomembrane, which was fabricated on the recipient substrate before fabricating gratings on it.

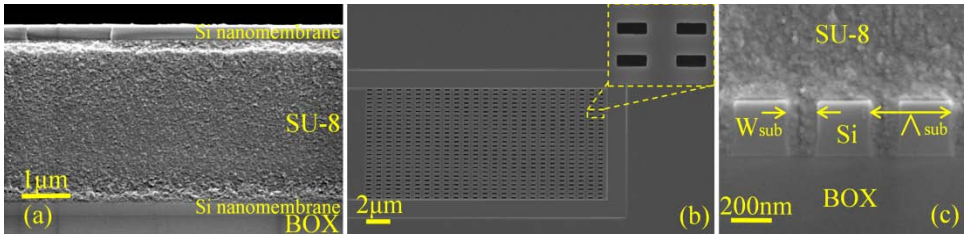

Figure 4-6 (a) A cross-sectional SEM image of the fabricated double-layer silicon nanomembranes, (b) a SEM image of the fabricated grating 2 before adhesive bonding, (c) a cross-sectional SEM image of the subwavelength nanostructure on the bottom layer showing SU-8 filling the etched holes.

DEVICE CHARACTERIZATION

The testing setup is shown in Figure 4-3. Input light is from a broad band amplified spontaneous emission (ASE) source with TE polarization. Output light is fed into an optical spectrum analyzer for analysis. The measured fiber-to-fiber coupling efficiency normalized to the light source is shown in Figure 4-7(a), which is a combination of the coupling efficiencies of the intra-layer grating couplers (grating 1 and grating 4) and the coupling efficiency of the inter-layer grating coupler (grating 2 and grating 3). In order to extract the coupling efficiency of the inter-layer grating coupler, it is necessary to measure the coupling efficiency of grating 1 and grating 4 first.

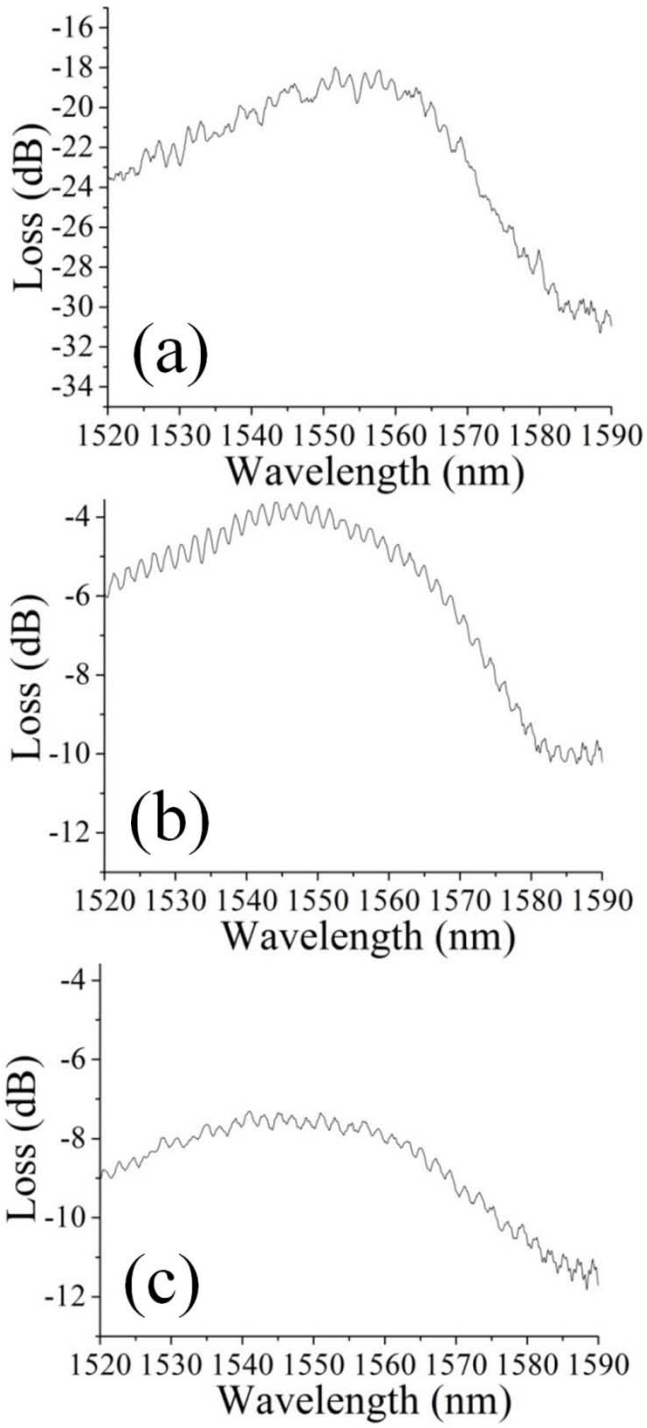

Figure 4-7: (a) Measured coupling efficiency of all four gratings combined as shown in Fig. 1, (b) measured coupling efficiency of grating 1, (c) measured coupling efficiency of grating 4.

The testing setup to measure grating 1 and grating 4 is shown in Figure 4-8. One pair of grating couplers was fabricated on different layers. Assuming equal coupling efficiencies for both input and output grating couplers, and negligible loss of linear tapers and connecting waveguides, the coupling efficiencies of grating 1 and grating 4 are extracted, as shown in Figure 4-7(b) and 4-7(c), respectively. The peak efficiency for grating 1 was measured to be 18% (-7.4 dB) at 1550 nm wavelength, and the peak efficiency for grating 4 was measured to be 44% (-3.6 dB) at 1550 nm wavelength. Note that the input and output fiber tilting angles were adjusted to be 14° and 10° from normal incidence for grating 1 measurement and grating 4 measurement, respectively, so that the grating peak efficiency appeared near 1550 nm wavelength. We also used 14° and 10° as input fiber tilting angle and output tilting angle, respectively, in the testing setup shown in Figure 4-3. The efficiency of grating 1 was lower than the simulated value. This is because the silicon nanomembrane above grating 1 was etched in the RIE to define devices on top layer. The SU-8 layer was exposed to RIE during the over-etching of silicon nanomembrane, and also exposed to the EB resist remover during resist removal. The SU-8/air interface is thus very rough, and causes random scattering at the interface.

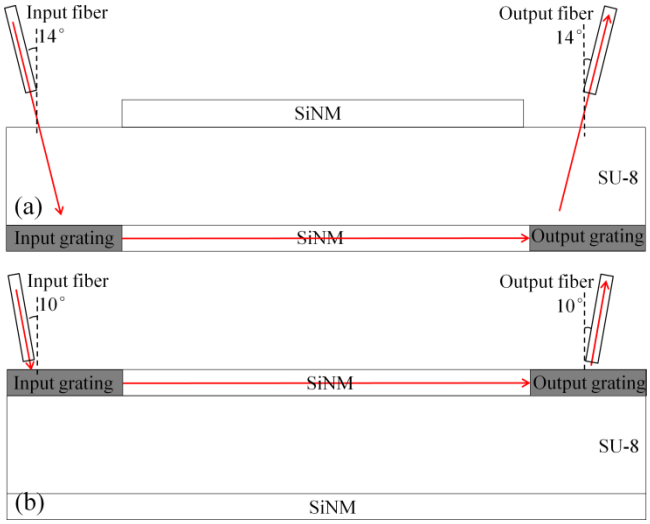

Figure 4-8: Testing setups to measure (a) grating 1, (b) grating 4.

Assuming negligible loss for linear tapers and connecting waveguides, we extracted the coupling efficiency of the inter-layer grating coupler by subtracting the coupling efficiencies of grating 1 and grating 4 from the coupling efficiency of all four gratings combined, as shown in Figure 4-9(a). The peak efficiency for the inter-layer grating coupler was measured to be 25% (-6.0 dB) at 1560 nm wavelength with a 3dB bandwidth of 41 nm. The simulated coupling efficiency is also shown in Figure 4-9(a). The peak wavelength shift is possibly due to fabrication errors. Comparing to the simulated result, the experimental result shows a higher peak efficiency but a lower bandwidth, because of the local maxima and minima probably induced by reflections between the two silicon nanomembranes [24]. We experimentally varied ΔL (as defined in Figure 4-3 and 4-4) over several samples and measured their coupling efficiencies at the target wavelength of 1560 nm. The efficiency drop is less than 1 dB when ΔL=12.0 +/- 0.1 μm, as shown in Figure 4-9(b), which means the misalignment-induced efficiency drop can be controlled within 1 dB with the EBL system.

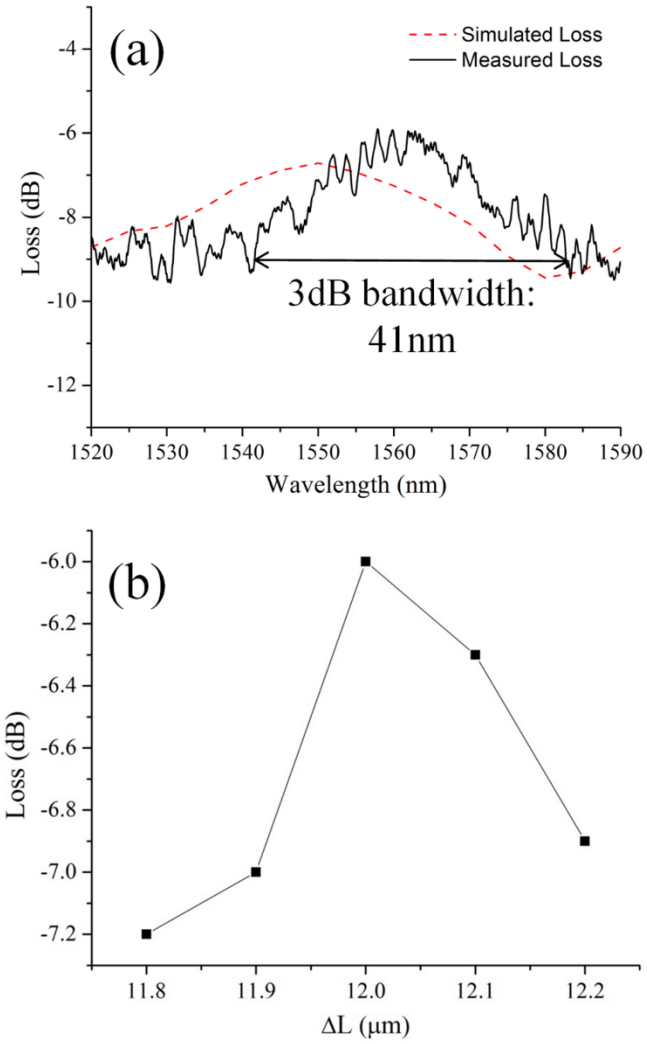

Figure 4-9: (a) Simulated and measured coupling efficiencies of the inter-layer grating coupler, (b) experimental inter-layer grating coupler efficiency at 1560 nm wavelength with different ΔL value.

SUMMARY

In conclusion, we presented a fabrication process flow to fabricate double-layer, on-chip, single crystalline silicon nanomembranes. We demonstrated simultaneous coupling to separate photonic layers using subwavelength nanostructure based intra-chip grating couplers. The peak coupling efficiency to the bottom (top) layer is 17% (44%) at 1557 nm (1555 nm) operating wavelength with TE polarization. We also demonstrated an

on-chip subwavelength nanostructure based inter-layer grating coupler with a peak efficiency of 25% at 1560 nm operating wavelength with TE polarization and a 3dB bandwidth of 35nm. This approach serves as a new platform for 3D photonic integrationg and novel 3D photonic devices, such as optical phased arrays (OPAs) [27].

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Chapter 5: 1-to-32 H-tree Optical Distribution on Adhesively Bonded Silicon Nanomembrane

INTRODUCTION

On-chip optical interconnects offers potential benefits compared to the conventional metal interconnects in the continuing trend toward higher bandwidth in advance VLSI circuits. Optics can deliver particularly precise timing of signals because of the low dispersion in optical channels, which is ideal for clock signal distribution [1-3]. Silicon photonics, in which wavelength-parallel optical data with terabit-per-second data rates can be transported through crystalline silicon waveguides or silicon nitride waveguides [4-5] over the entire chip, is considered a promising solution to overcome the predicted limitations in metallic interconnects [6]. On-chip optical clock distribution using an H-tree structure has been demonstrated on the silicon-on-insulator (SOI) platform [7-8]. However, these demonstrations limit the optical clock distribution network and the electronic components to the same layer. In order to maximize the design flexibility of an optical clock distribution network, it is preferable to stack photonic layers vertically on other electronic layers. Comparing to depositable silicon nitride platform [3, 9-11], single-crystalline nanomembrane offers denser integration density, as well as the possibilities to achieve high-speed photonic integrated circuit (PIC) without using additional layers for active devices. In previous chapters, methods to stack additional silicon nanomembranes onto existing chips have been demonstrated using transfer printing and adhesive bonding. Although both methods have their pros and cons, adhesive bonding is currently the only approach to fabricate large (cm X cm) defect-free stackable silicon nanomembranes.

In this chapter, we present the experimental demonstration of a 1-to-32 H-tree optical distribution network on adhesively bonded silicon nanomembranes. The

fabricated H-tree structure shows low insertion loss, which is comparable to similar structure fabricated on SOI, uniform outputs and large optical bandwidth. Using the presented method, high-performance optical clock distribution network can be vertically integrated onto existing PICs.

DEVICE DESIGN

The optical distribution from 1 input to 32 outputs follows an H-tree geometry, in which the waveguide lengths, the number of 90° bends and splitters are identical for the input to each outputs of the optical distribution. Strip silicon waveguides with a cross-sectional dimension of 500 nm X 250 nm are used, which provide stronger light confinement compared to shallow etched rib waveguides. Propagation losses of around 3.1 dB/cm in the wavelength range from 1535 nm to 1565 nm have been demonstrated for SOI based single mode waveguides with a cross-sectional dimension of 500 nm X 250 nm [12], using the processing equipments at UT-Austin Microelectronic Research Center.

The H-tree geometry includes compact Y-splitters based on arc-shaped branching waveguides [13]. This kind of 1-to-2 splitter is not sensitive to refractive index variations due to temperature and/or thickness variations of silicon layers and also insensitive to unwanted residues and air voids in the junction region comparing to Y-splitters based on straight branching waveguides. The radii of the arcs are chosen to be 10 μm to avoid significant bending loss [14]. This value is also used in the 90° bends in the H-tree geometry.

Using the strip waveguides, Y-splitters based on arc-shaped waveguides and the 90° bends described above, a 1.1 cm long 1-to-32 H-tree optical distribution has been designed, and a schematic is shown in Figure 5-1. The 32 outputs cover an area of 4 mm

X 4 mm. In order to perform optical characterization, subwavelength nanostructure based grating couplers described in ref. [15] with 900 μm linear tapers are connected to both input waveguide and output waveguides to couple light in and out of the H-tree structure. All output waveguides are folded to align in one direction to simplify alignment between the grating couplers and optical fibers.

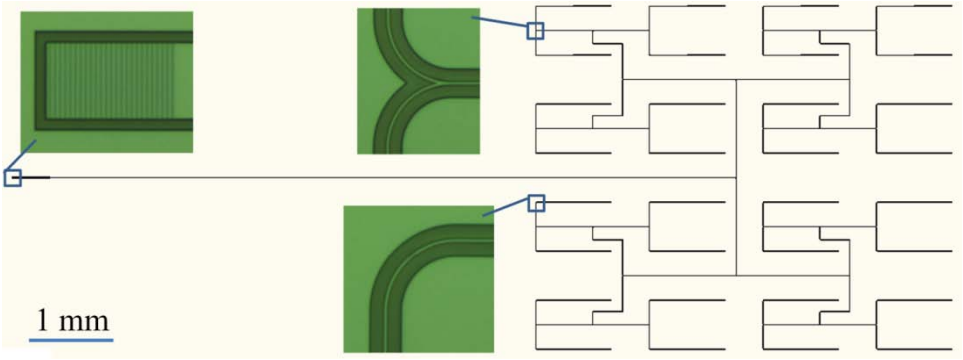

Figure 5-1: Schematic of the H-tree optical distribution with 1.1cm long strip waveguides, five Y-splitters, three 90° bends and two grating couplers with linear tapers. Optical microscope images of grating coupler, Y-splitter and 90° bend are inserted.

DEVICE FABRICATION

The process flow is shown in Figure 5-2. The entire material stack from top to bottom contained an 18 mm X 18 mm SOI chip, a 1.5 μm SU-8 layer coated on the silicon device layer, another 1.5μm SU-8 layer coated on the silicon device layer of a 20 mm X 20 mm SOI chip, and a 20 mm X 20 mm SOI chip. The two SOI chips are both from a SOI Unibond 150 mm wafer manufactured by SOITEC with a 250 nm thick lightly p-doped silicon layer and a 3μm BOX layer. Before bonding, the two SOI chips were thoroughly cleaned in piranha solution. The native oxide was removed with buffered oxide etch (BOE) solution. Both the chips were dehydrated before applying SU-8 layer. Next, a 1.5 μm thick SU-8 layer was spun onto the SOI chips, and soft baked at 95 °C to evaporate extra solvent. Then, the smaller (18 mm X 18 mm) SOI chip was put

upside down on the larger (20 mm X 20 mm) SOI chip. Pressure was applied through a home-made bonder, which is shown in Figure 5-2(b). The material stack was mounted between two thick Pyrex glass slides. The steel ball and the Belleville washer spread the point force generated by the thumb screw onto the thick Pyrex glass plate, forming a gradient pressure distribution. This pressure distribution avoided the formation of air cavities in between the two SU-8 layers. The thermal expansion of Belleville washers also compensated pressure decreasing induced by the reflow of the polymer. The sample was kept in a 90 °C oven for 24 hours to let polymer reflow and squeeze out the trapped air bubbles. The bonded SOI chips are shown in Figure 5-2(c).

After bonding, the silicon handle of the top SOI chip was mechanically polished down to ~100 μm, as shown in Figure 5-2(d). This remaining silicon handle was removed by DRIE, as shown in Figure 5-3(e). A detailed description of the recipe used in DRIE can be found in ref. [12]. The silicon etch rate was around ~5 μm/min. To control the thermal budget of the DRIE process, the ~20 min etch process is divided into five 5-minute long periods. The tool was cooled down for 1 minute between two periods to let heat be dissipated. With the selectivity of ~80 for silicon to oxide, the 3 μm BOX of the top SOI chip was used as a stopping layer to protect the silicon nanomembrane underneath.

After DRIE, the top SOI chip without silicon handle became transparent to ultraviolet light. The sample was illuminated by 365 nm ultraviolet light through the top SOI chip to crosslink the SU-8 polymer. A 12-hour post exposure bake at 65 °C was done to further crosslink the SU-8. Baking at a low temperature helped minimizing the strain, as the thermal expansion coefficients of silicon and SU-8 are different. After that, the BOX of the top SOI chip was removed by HF wet etching, leaving a 250 nm thick silicon

nanomembrane adhesively bonded to the bottom SOI chip for device fabrication, as shown in Figure 5-2(f).

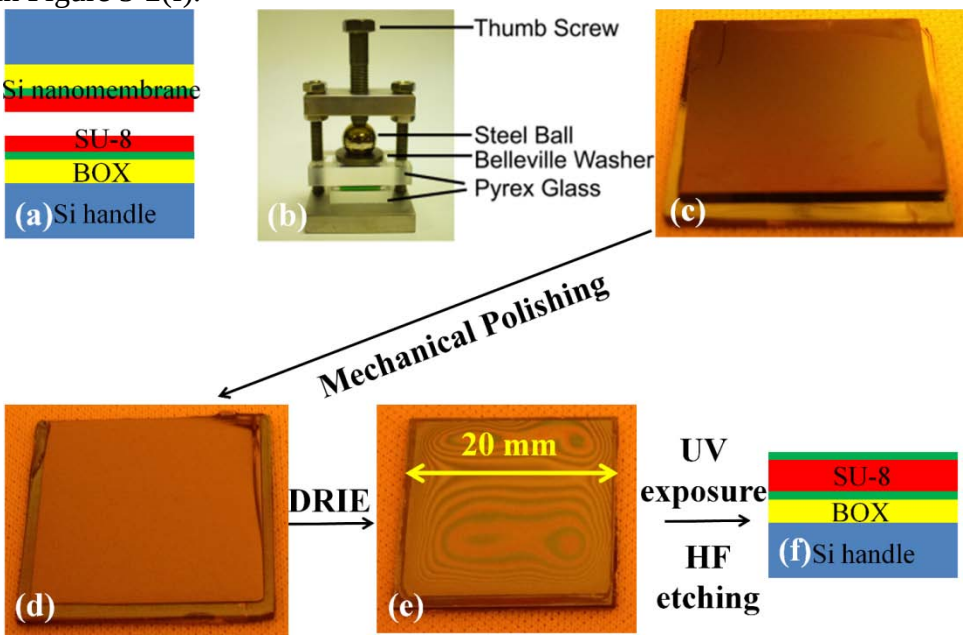

Figure 5-2: The process flow for bonding silicon nanomembrane onto another SOI chip, (a) schematic of the material stack structure, (b) the home-made bonder used for adhesive bonding, (c) the bonded two SOI chips, (d) polishing the silicon handle to ~100 μm, (e) removing the remaining silicon handle with DRIE, (f) schematic of a silicon nanomembrane bonded to a SOI chip.

The adhesively bonded silicon nanomembrane can be patterned into the H-tree structures through lithography and etching steps. The sample was coated with ZEP-520A positive photoresist and exposed by electron beam lithography using JEOL 6000 system. The waveguides were defined by exposing two 2 μm wide air trenches on each side of the waveguides. One thing worth noting is that the prebake of photoresist was done in 90 °C oven for half an hour. This low prebake temperature is to ensure that the strain generated from prebake is minimized. The exposed sample was etched with HBr/Cl_2 based reactive ion etching (RIE). After etching, the sample was exposed to O_2 plasma in an RIE tool for 30s, followed by a bath in 90 °C remover PG, to remove the photoresist residue. Cross-

sectional scanning electron microscope (SEM) images of the adhesively bonded silicon nanomembrane, developed photoresist pattern of the subwavelength nanostructure on the adhesively bonded silicon nanomembrane and the etched subwavelength nanostructure on the adhesively bonded silicon nanomembrane are shown in Figure 5-3 (a-c), respectively. Top-view SEM images of the grating coupler and the Y-slitter are shown in Figure 5-3 (d-e), respectively.

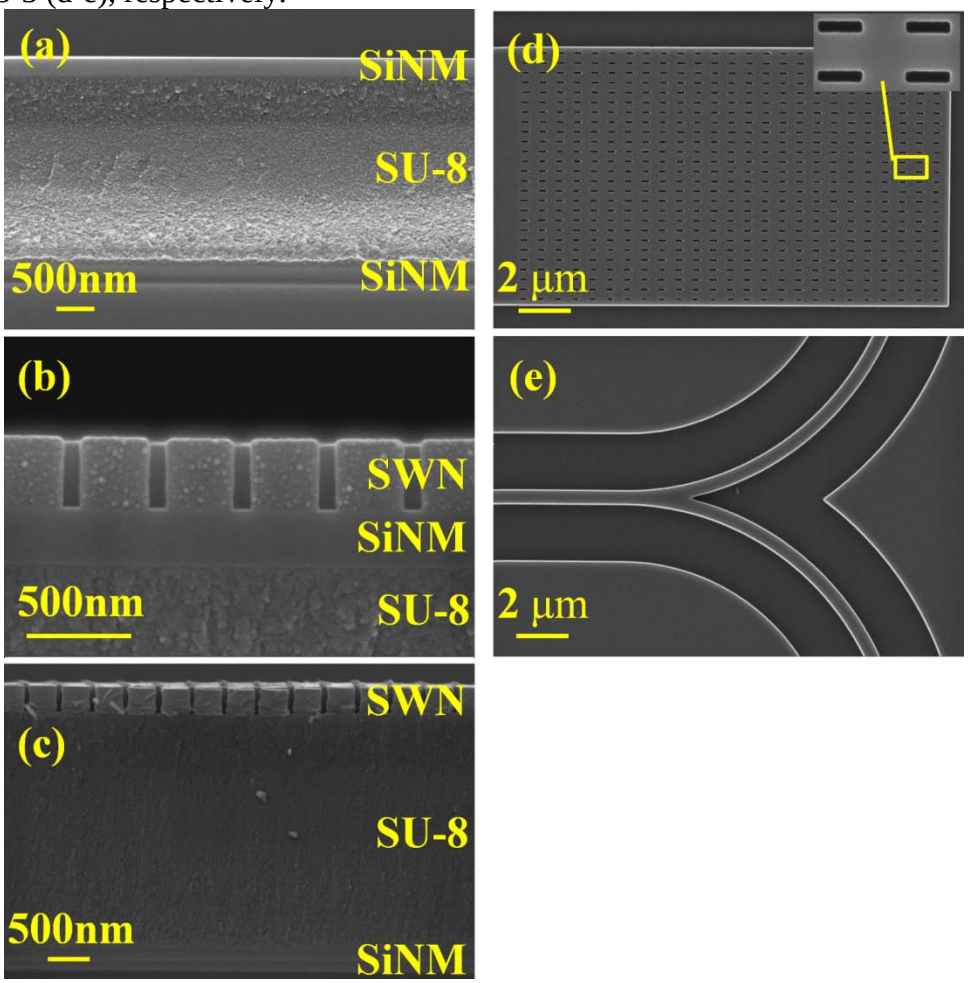

Figure 5-3: SEM images of (a) cross-section of a silicon nanomembrane (SiNM) adhesively bonded onto a SOI substrate, (b) cross-section of the photoresist pattern of the subwavelength nanostructure (SWN), (c) cross-section of the subwavelength nanostructure fabricated on the bonded silicon nanomembrane, (d) grating coupler, (5) Y-slitter.

LOSS CHARACTERIZATION

The propagation loss of 500 nm wide single-mode waveguides fabricated on the adhesively bonded silicon nanomembranes was measured using the cut-back method. Serpentine pattern with same the number of bends but different waveguide lengths (10 mm, 20 mm, 30 mm, 40 mm and 50 mm) were fabricated. Subwavelength nanostructure based grating couplers were utilized for input and output light coupling. A polarization maintaining fiber was used to couple transverse-electric (TE) polarized light at 1550 nm into the waveguides. The output light was collected by a single mode fiber and was measured by an optical power meter. The result is presented in Figure 5-4. The propagation loss of the single-mode waveguide on the adhesively bonded silicon nanomembrane is 4.3 dB/cm at 1550 nm wavelength. This value is 1.2 dB/cm higher than that of single-mode waveguides fabricated on SOI wafers. In order to investigate the source of this additional loss, the top surface roughness of the adhesively bonded silicon nanomembranes was measured using atomic force microscopy (AFM). The surface roughness of the adhesively bonded silicon nanomembrane was 0.629 nm, while it was 0.128 nm for SOI [12]. We conclude that the additional propagation loss is from the increased surface roughness of the adhesively bonded silicon nanomembrane. The propagation loss can be reduced by replacing our RIE with inductively coupled plasma (ICP) etching, which reduces the sidewall roughness of etched waveguides by lowering the required RF bias voltage.

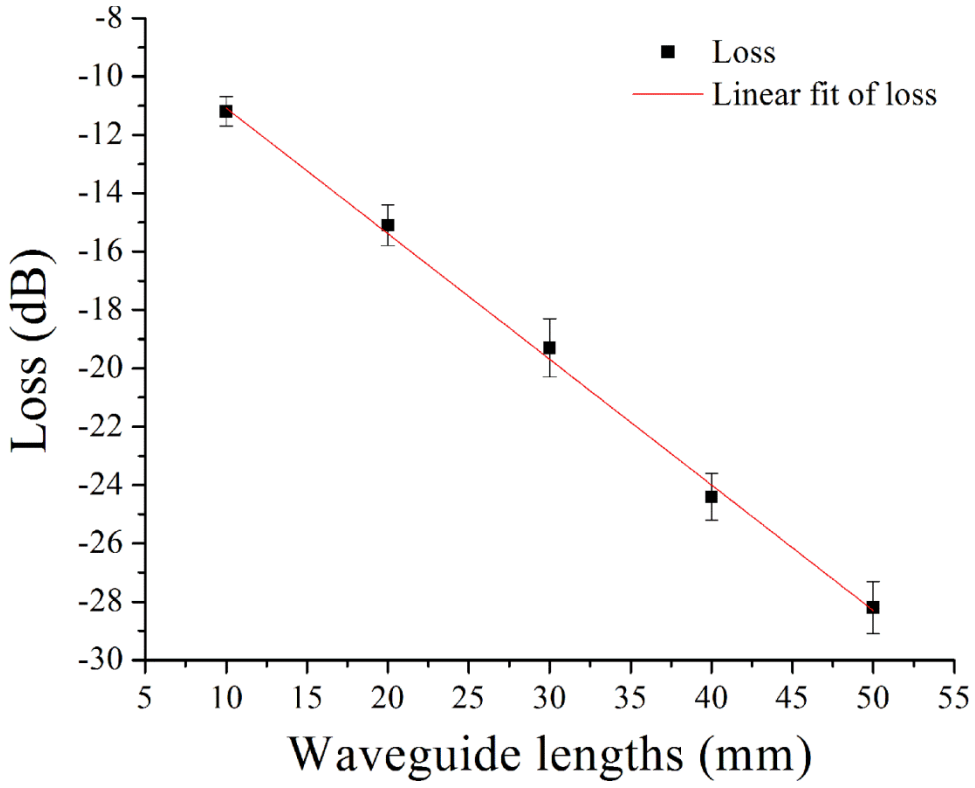

Figure 5-4: Propagation loss of single-mode waveguide on adhesively bonded silicon nanomebrane determined by varying waveguide lengths using the cut-back method.

In order to characterize the total excess loss of the H-tree optical distribution, TE polarized light was used as the input and a power meter was used to detect the output power from each output at 1550 nm wavelength. The total excess loss, which excludes the fiber-to-waveguide coupling loss and the waveguide propagation loss, is defined as $-\log[(\sum I_m)/I_{in}]$, where I_m is the intensity of the m^{th} output channel, and I_{in} is the output intensity of a reference waveguide on the same chip with the same input & output grating couplers and waveguide length as the H-tree structure. The excess loss of the H-tree optical distribution at 1550 nm wavelength is measured to be 2.2 dB, which is mainly from the excess losses of five 1-to-2 Y-splitters. The average excess loss per Y-splitter is 0.44 dB, which is comparable to the results presented in ref. [13].

The transmission spectrum of the H-tree optical distribution is also characterized. TE polarized light from a broadband amplified spontaneous emission (ASE) source was coupled to the H-tree structure through an input grating coupler, and the output light from one output of the H-tree structure was analyzed by an optical spectrum analyzer (OSA). The transmission spectrum obtained by normalizing the output signal to the light source is shown in Figure 5-5, which has a peak value of -29 dB at around 1550 nm wavelength. This -29 dB includes the coupling loss of two grating couplers, the excess losses of five Y-splitters, the waveguide propagation loss of the 1.1 cm single-mode waveguide and the fanout loss of a 1-to-32 geometry. The two grating couplers' transmission spectrum was obtained by the method described in ref. [16] and is shown in Figure 5-5. The grating coupler has a peak efficiency of 45% (-3.5 dB) at 1550 nm operating wavelength, which is comparable with the result described in chapter 4. Considering the excess loss of five Y-splitters to be 2.2 dB, the waveguide propagation loss to be 4.7 dB (4.3 dB/cm X 1.1 cm) and the fanout loss to be 15 dB, the transmission spectrum agrees well with our previous loss characterizations. We can see that the transmission spectra of grating couplers and H-tree optical distribution have similar profiles through an 80 nm bandwidth, meaning the Y-splitters and waveguide have nearly constant loss in C-band and L-band. The H-tree's spectrum has more obvious fluctuations, which may result from the polarization dependence of the Y-splitters [13].

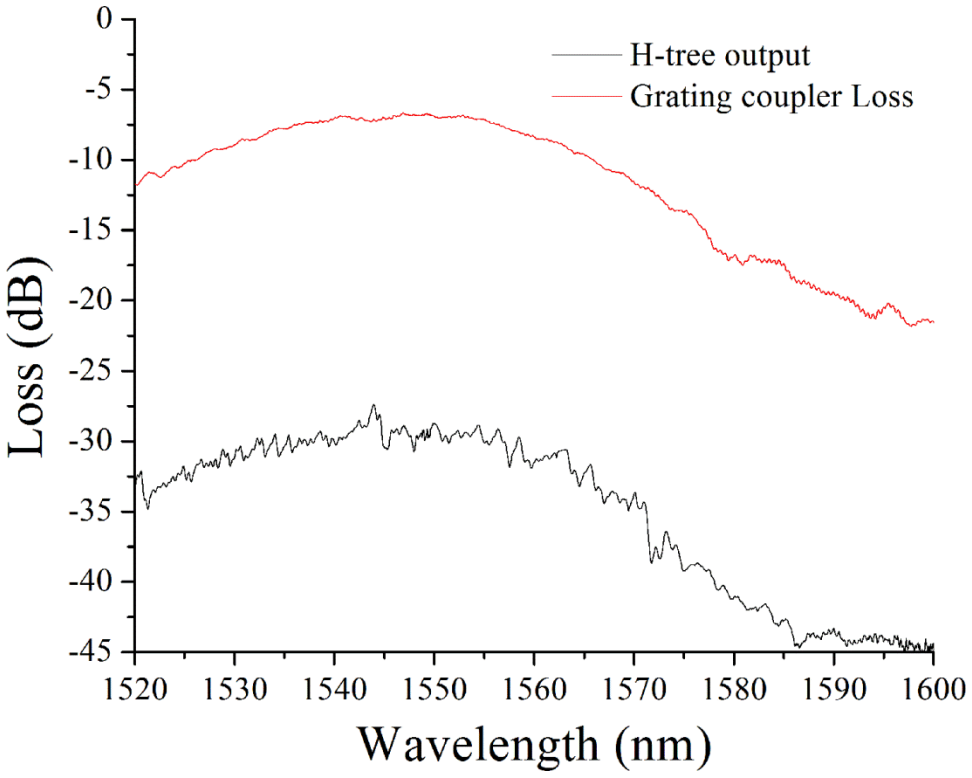

Figure 5-5: Transmission spectra of the H-tree optical distribution (black) and the two grating couplers for input and output (red).

DEVICE CHARACTERIZATION

A top-down IR-image of the entire optical distribution is shown in Figure 5-6(a). At each output of the optical distribution, TE polarized light at 1550 nm wavelength was coupled out of the grating coupler and the near field image was collected by an IR CCD camera suspended above the grating coupler. The observation clearly shows 32 outputs. Quantitative measurements of the intensities from each output were performed to characterize the uniformity of this H-tree optical distribution, as shown in Figure 5-6(b). The uniformity, which is defined as $10\log(I_{max}/I_{min})$, is calculated to be 0.72 dB.

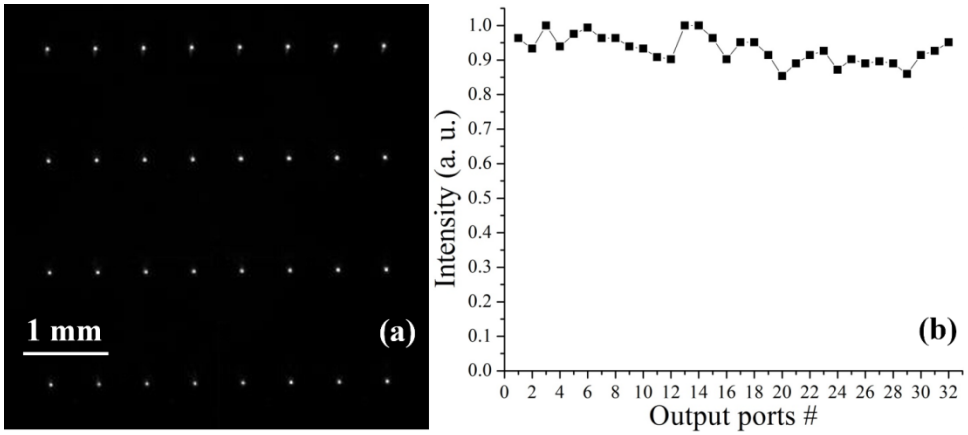

Figure 5-6: (a) A top-down IR-image of the 1-to-32 optical distribution, (b) Measured intensities from each outputs of the H-tree structure.

The bandwidth of the H-tree optical distribution was characterized by optical autocorrelation as described in ref. [17]. In order to obtain enough optical signal for autocorrelation, a testing waveguide, which has the exact geometry and dimensions as one arm of the H-tree structure (including input & output grating couplers with linear tapers, 1.1cm single-mode waveguide and eight 90° bends), was used. A TE polarized optical pulse generated from a femtosecond laser with a center wavelength of 1550 nm was launched into the device through a polarization maintaining fiber. The output power is collected by a single-mode fiber, amplified by an erbium doped fiber amplifier (EDFA), and finally fed into an autocorrelator. The input and output optical pulses in time domain are shown in Figure 5-7(a). The intensity of the output pulse is normalized to the intensity of the input pulse. The output pulse is broadened in the time domain after going through the testing structure. The frequency domain responsivity of the input and output pulses, obtained by the fast Fourier transform of the pulses in time domain, are shown in Figure 5-7(b). The 3 dB bandwidth of the device is found to be 880 GHz. The bandwidth limiting factor is not the dispersion of the single-mode waveguide, but the optical nonlinearities induced by the high peak power of the femtosecond pulse [18], and

the dispersion of the grating couplers. The bandwidth could be larger because the average power of an optical link is much lower than the peak power of the femtosecond pulse.

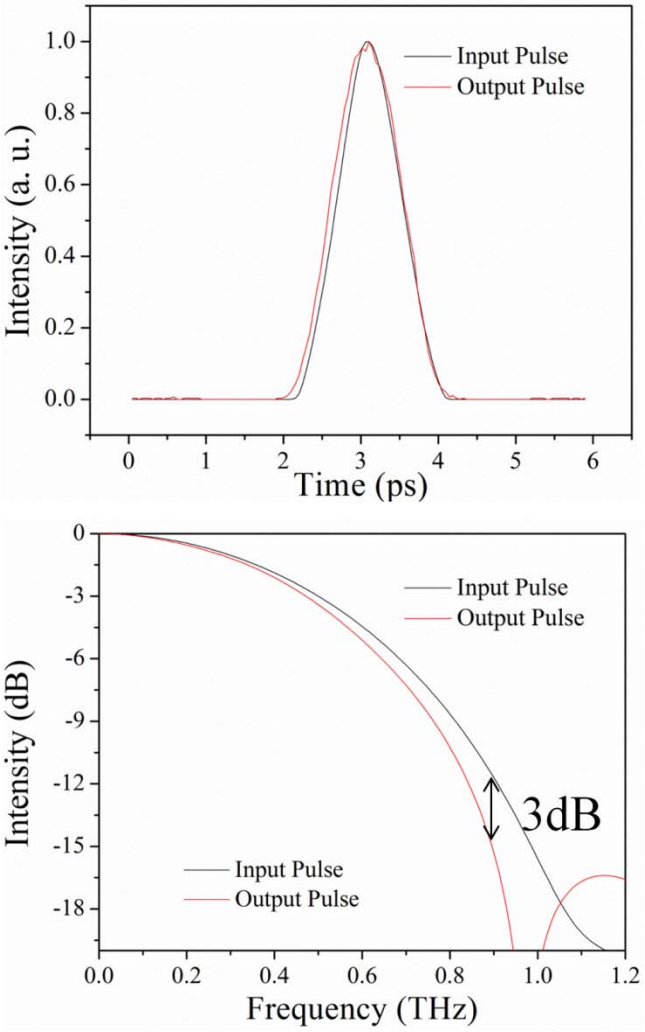

Figure 5-7: (a) Input and output pulses in the time domain, (b) input and output pulses in the frequency domain.

SUMMARY

In summary, a 1-to-32 H-tree optical distribution network was fabricated on adhesively bonded silicon nanomembrane. The single-mode waveguides fabricated on this platform has a propagation loss of 4.3 dB/cm, which is comparable to waveguides

fabricated on SOI. The H-tree structure has an excess loss of 2.2 dB, induced by Y-splitters, and output uniformity of 0.72 dB. This grating-coupled H-tree structure has a 3 dB bandwidth of 880 GHz measured by autocorrelation, which is sufficient to support the interconnect bandwidth requirement in future VLSI chips.

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Chapter 6: Ultra-Low Loss Silicon Waveguide Crossing Using Bloch Modes in Index-Engineered Cascaded Multimode Interference Couplers

INTRODUCTION

Efficient waveguide crossings are required to materialize the full potential of silicon photonics for on-chip optical interconnects. Single mode silicon waveguide crossings with normal intersections result in over 1 dB insertion loss and ~-10 dB cross-talk due to the high index contrast of the silicon-on-insulator (SOI) platform [1, 2]. Subwavelength gratings in silicon waveguides have been used to lower the effective refractive index at the crossing resulting in insertion loss as low as 0.023 dB and <-40 dB cross-talk [1]. However, this structure requires ~10 μm long adiabatic tapers to gradually reduce the effective refractive index with near 0.3 dB loss per taper. Also, the reduced effective refractive index (<2) is accompanied by the mode profile extending several microns laterally, which in turn increases the waveguide pitch in a cross-grid. As another approach, low-Q resonator based crossings suffer from limited optical bandwidth (10-15 nm) [3]. On the other hand, multimode interference (MMI) based crossings with relatively compact size (13x13 μm^2) have been demonstrated with insertion loss of ~0.2 dB [2] [4]. In this type of structures, the self-focusing effect of the MMI is used to form a single image of the MMI input waveguide mode profile at the crossing thus minimizing the effect of the crossing waveguide on the mode profile. Recently, it was theoretically (using 2D finite difference time domain (FDTD) simulations) shown that a periodic structure formed by cascading multimode focusing sections can support a low-loss Bloch wave [5]. In addition to the fact that this structure can potentially lower the insertion loss to 0.04 dB per crossing, a waveguide pitch <3 μm also enables compact waveguide crossing arrays. In this paper we show that a compact periodic structure formed by cascading MMIs with engineered lateral cladding refractive index can lead to less than

0.01 dB insertion loss per crossings, making possible for integrating 100s of waveguide crossings with minimal insertion loss and cross-talk.

DEVICE DESIGN

The platform is a SOI substrate with 3μm thick buried oxide (BOX) layer and 250 nm thick top silicon layer (n_f=3.47). A schematic of the waveguide array crossing structure is shown in Figure 6-1(a-b). This arrayed structure may be thought as cascading several MMI based waveguide crossing shown in Figure 6-1(c), in which, according to the self-imaging principle of multimode waveguides, images of the input field are periodically formed. It has been proposed that the multimode waveguide can be crossed by another one at the points where single-fold images are formed.

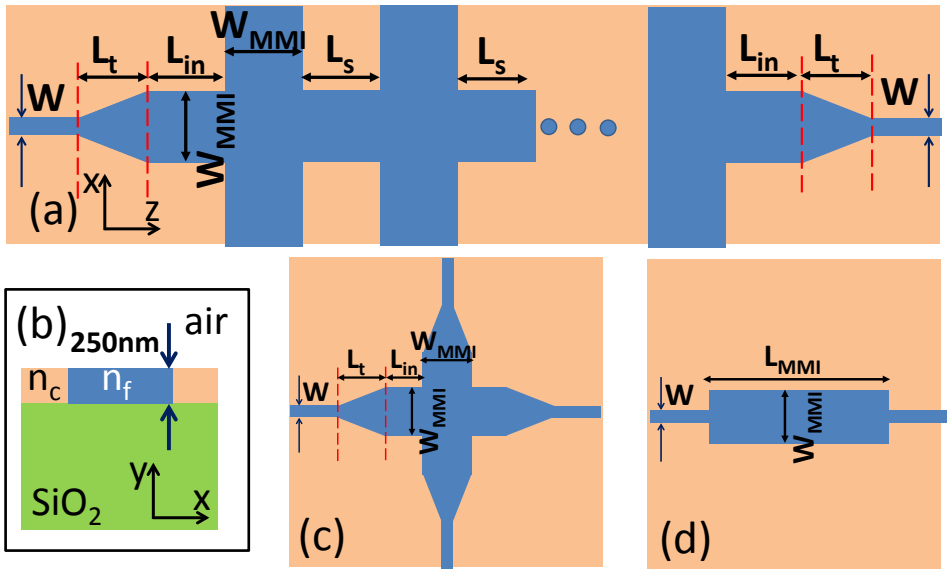

Figure 6-1: (a) A top view schematic of the cascaded multimode interference based waveguide crossings, (b) a side view schematic of the waveguide structure with lateral cladding indicated, (c) a single waveguide crossing structure, (d) a 1×1 MMI.

In order to design a low-loss waveguide crossing array, we first investigate the loss mechanism in a simple 1×1 symmetric MMI structure shown in Figure 6-1(d). Similar to the previously reported designs, here we assume the multimode waveguide width, W_{MMI}=1.2 μm, and input/output single mode waveguide width, W=0.6μm. Note that the MMI region only supports 3 modes (TE polarized). So far, the MMI insertion loss has been explained by the modal phase errors [6-8]. For an ideal self-imaging it is required that $\beta_{m,ideal} = \beta_0 - m(m+2)\pi/3L_\pi$, where β_m the propagation constants of mode m, and L_π is the beat length of self-imaging process [9]. However, following the analysis [6] one can write:

$$\beta_m = \beta_0 \sqrt{1 + \frac{K_{To}^2 - K_{Tm}^2}{\beta_0}} \tag{1}$$

where, $K_{Tm}=(m+1)\pi/W_{em}$ is the transverse wave number of mode m, and W_{em} is the effective width of the MMI for the m^{th} mode. The modal phase error is given as $\Delta\varphi_m = L_{MMI}\Delta\beta_m = L_{MMI}(\beta_m - \beta_{m,ideal})$, where L_{MMI} is the MMI length. It has been shown that the lateral cladding index (n_c) [see Figure 6-1(b)] can be tuned to minimize $\Delta\varphi_m$ for a few number of dominant modes, particularly, given at N-folding imaging length [6]:

$$\Delta\varphi_m \approx (P/4)\frac{\lambda_0^2(m+1)^4\pi}{2Nn_f^2W_{e0}^2}\left[\frac{1}{8} - \frac{\lambda_0 n_{f2D}^2}{6\pi W_{e0}(n_{f2D}^2 - n_{c2D}^2)^2}\right] \tag{2}$$

where, λ_0 is the optical wavelength and P is the number of self-imaging periods. We added the multiplier P/4 to the modal phase error presented in [7], since we have a symmetric interference here (required MMI length is divided by 4 [8]), and P=2 in the MMI crossing structure. Also, we note that n_{f2D}=2.9 and n_{c2D} are the effective refractive indices of the fundamental mode of an infinite slab waveguide with the same thickness as the MMI (250 nm) and core refractive index of n_f and n_c, respectively. While tuning the

lateral cladding index (nc) is generally applicable to MMIs that support several modes in their multimode region, we notice that the multimode waveguide shown in Figure 6-1(d) only supports 3 modes (0^{th}, 1^{st} and 2^{nd}), among which the odd 1^{st} order mode is not excited to due to the symmetry of the structure. That leaves only 2 modes (m=0 and m=2), for which the self-imaging condition is simply reduced to:

$$\beta_0 - \beta_2 = 2\pi n / L_{MMI}, \text{ n: integer} \quad (3)$$

One notes that for any W_{MMI} and n_c, as long as only the 0^{th} and 2^{nd} modes are excited, there is always an MMI length for which this condition can be perfectly satisfied. In other words, remaining phase error ($\Delta\varphi_2$) can be eliminated by tuning L_{MMI}.

In order to confirm this observation, we simulate different 1×1 MMI structures shown in Figure 6-2(a-c) using 3D PhotoDesign FIMMPROP, an eigenmode decomposition based simulator. Linear tapers (Lt=1 μm) are used in Figure 6-2(b-c) for high transmissions as suggested by Chen et al [4]. In each case, we sweep the MMI lengths, L_{MMI}, L, L_{in} for MMIs shown in Figure 6-2(a-c), respectively, and find the maximum transmission. Figure 6-2(d) shows optical transmission as a function of n_c.

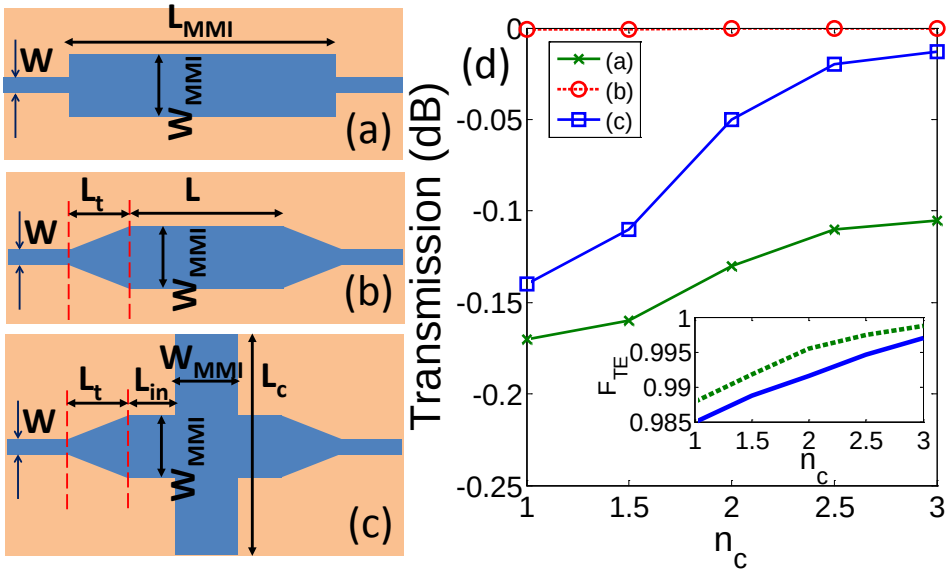

Figure 6-2: Schematics of simulated structures, (a) 1×1 MMI with single mode access waveguides, (b) 1×1 MMI with tapered input output transitions, (c) MMI waveguide crossing using 1×1 MMI with tapered input output transition, (d) simulated transmission versus lateral cladding index (n_c) for the structure in (a-c), (d) inset shows TE fraction versus n_c for the fundamental mode in the single mode access waveguide (width=0.6 μm, solid blue curve) and the second order mode in the MMI region (width=1.2 μm, dashed green line).

As n_c increases, the transmission improves in all cases. Interestingly, the 1×1 MMIs with tapers and without crossing are essentially loss-less and the 1×1 MMIs without tapers have the worst performance. Since the modal phase errors are not applicable in any of these cases, we need to consider another loss mechanism.

In the structure shown in Figure 6-2(a), we note that the fundamental mode in the single mode access waveguide, and the 2nd order mode in the multimode region are both quasi TE modes with considerable amount of TM polarization (~1%) for n_c=1 as shown in inset of Figure 6-2(d). Here, the TE (TM) fraction is the fraction of the Poynting vector with horizontal (vertical) electric field:

$$F_{TE} = \frac{\int E_x H_y ds}{\int P_z ds} \tag{4}$$

As n_c increases, both of these modes becomes essentially completely TE and power transmission between the two waveguides improves at the input and output. The tapers help improving the power transmission by avoiding sharp transitions and by reducing the portion of the power in the 2^{nd} order mode in the multimode region [4].

Similarly, when we compared tapered MMIs with and without waveguide crossings, we note that the crossing section is much wider compared to the MMI width ($L_c >> W_{MMI}$), this section can be thought of as slab waveguide. When n_c increases from 1 to 2.5, both excited modes in the MMI region become pure TE, the power transmission between the two section increases.

Thus we claim that the losses in the 3-moded MMI structures are due to coupling losses at sharp transitions and not due to modal phase errors. We also simulate the structures shown in Figure 6-3(a-c) to support this claim. Table 1 shows the modal field excitation coefficients, c_m, at the outputs (right sides) of the structures shown in Figure 6-3(a-c). c_m values are normalizes normalized with respect to the input power and are calculated using overlap integrals [9].

Table 6-1: The modal field excitation coefficients c_m in the 3-mode sections (width=W_{MMI}) in Fig(a) and (b) and in the crossing section (width=L_c) in Fig(c), L_c=4μm in our FIMMPROP simulations. The total number of modes, M, is 3 at the outputs of the structures in Fig(a) and (b). M=19 at the output of the structure in Fig(c).

		Figure 6-3(a)	Figure 6-3(b)	Figure 6-3(c)
n_c=1	$\lvert c_0\rvert^2$	0.828	0.996	0.475
	$\lvert c_2\rvert^2$	0.155	0.004	0.326
	$\sum_{m=0}^{M-1}\lvert c_m\rvert^2$	0.983	~1	0.991
n_c=2.5	$\lvert c_0\rvert^2$	0.897	0.949	0.520
	$\lvert c_2\rvert^2$	0.096	0.051	0.312
	$\sum_{m=0}^{M-1}\lvert c_m\rvert^2$	0.993	1	0.998

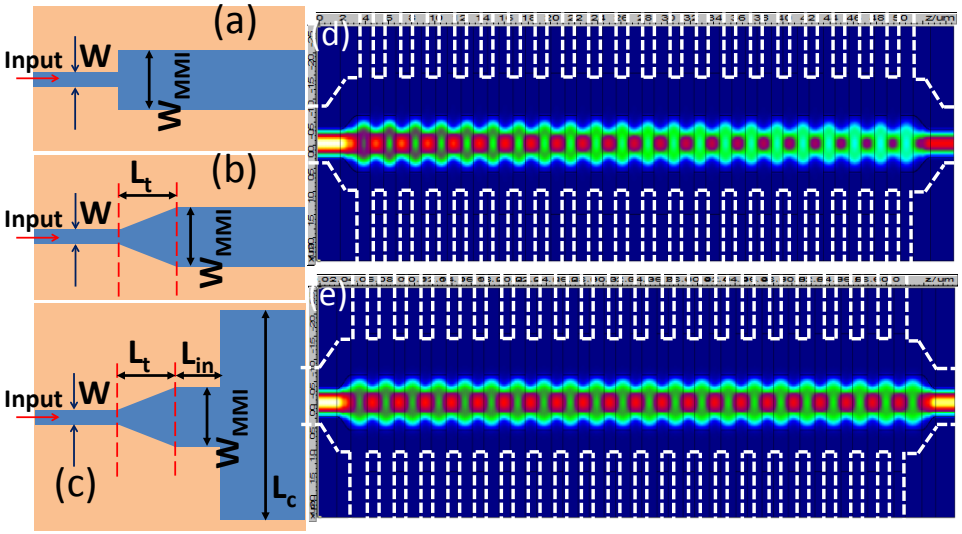

Figure 6-3: (a-c) simulated structures for investigation of coupling efficiencies into the 1×1 MMI shown in Fig (a-c). Simulated waveguide crossing arrays for (d) n_c=1, L_{in}=1.35 μm, L_s=1.04 μm and (e) n_c=2.5. L_{in}=2.27 μm, L_s=1.88 μm.

One notes that the power transmission from the input single mode waveguide into the multimode region has about 2% loss in the 1×1 MMI with n_c=1 and without the input taper. This loss is reduced to less than 1% when n_c is increased to 2.5. Using the input taper makes the coupling from the single-mode input into the multimode waveguide nearly loss-less regardless of n_c. Inserting the waveguide crossing section intrudes some loss due to sharp transitions between waveguide sections, where one of one side supports a quasi TE mode with a significant TM fraction. Increasing nc reduces the TM fraction to 0 and increases the overall power transmitted into the supported modes at the output.

Thus, for large number of waveguide crossings it is imperative to increase the n_c to at least 2.5 where the curve of transmission versus n_c reaches the point of diminishing returns. We simulated the structure shown in Figure 1(a). Figure 6-3(d) and (e) show the propagation field profiles inside with 20 crossings, for n_c=1 and n_c=2.5, respectively. The insertion loss is 0.11 dB and 0.008 dB per crossing in Figure 6-3 (d) and (e), respectively. In these simulations, we first maximize the transmission for the structure with 20 crossings, and find L_{in}=1.35 μm, L_s=1.04 μm for n_c=1 and L_{in}=2.27 μm, L_s=1.88 μm for n_c=2.5.

DEVICE FABRICATION AND CHARACTERIZATION

We fabricated waveguide arrays vertically crossed by other waveguide arrays as shown in Figure 6-4(a) using both conventional MMI crossings and index-engineered MMI crossings. In order to implement n_c>1, subwavelength nanostructure (SWN) is used to engineer the lateral cladding refractive index [7]. The SWN is periodic along the light propagation direction, and its refractive index (n_{SWN}) can be engineer by tuning the filling factor (ff) of air trench inside the SWN, which is defined as the ratio between air trench width (W) and SWN period (Λ). We used Λ=200 nm for the SWN, and we fabricated

devices with W=30, 40, 50, 60, 70 and 80nm. The width of the SWN is 200 nm to accommodate the field penetration into the lateral cladding.

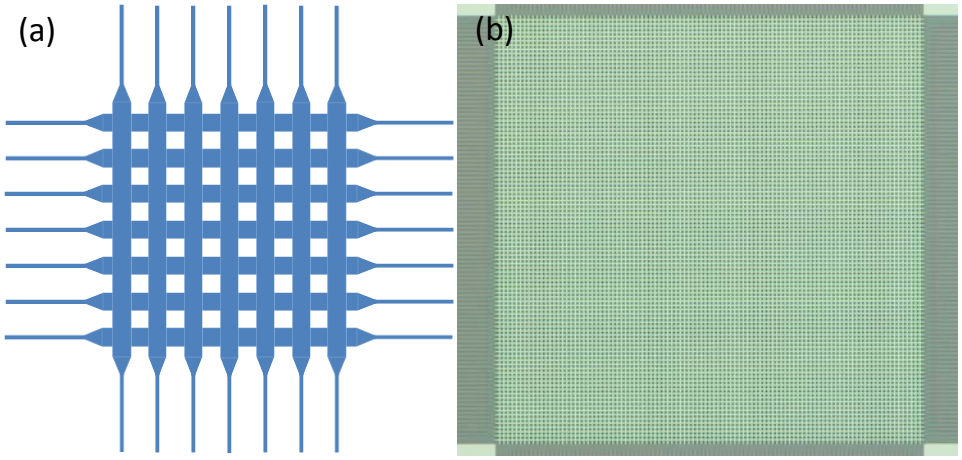

Figure 6-4 (a) Schematic of a cross-grid MMI based waveguide array crossing. 7×7 cross-grid is shown for simplicity, (b) an optical microscope image of the fabricated 101×101 cross-grid.

The designed structures were fabricated on a SOI wafer using electron beam lithography (EBL) and reactive ion etching (RIE). MMI crossings with and without SWN are used in the cross-grids for comparison. Figure 6-4(b) shows an optical microscope image of the fabricated 101×101 cross-grid with index-engineered MMI crossings. Figure 6-5(a-b) and (c-d) show scanning electron microscope (SEM) images of the MMI crossings, with and without SWN, respectively.

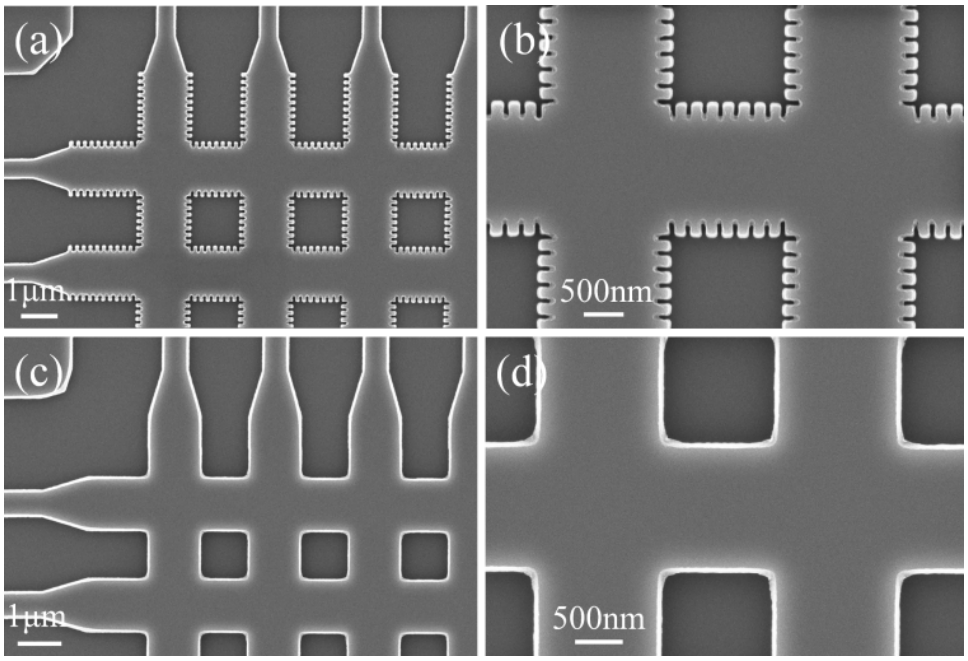

Figure 6-5: SEM images of the fabricated waveguide array crossings with (a-b) and without (c-d) index engineering of the lateral claddings.

Transverse electric (TE) polarized light from a broad band amplified spontaneous emission (ASE) light source was coupled in and out of the cross-grid using SWN based grating couplers [10]. The transmissions obtained from the cross-grid were normalized to the transmission of a reference waveguide with the same propagation length. We experimentally found that the index-engineered MMI crossing with W=50 nm had the best performance. Figure 6 shows the normalized transmissions of the 101x101 cross-grids for a horizontal waveguide in the middle of the grid (the 51th waveguide) with both the index-engineered (n_c=2.5, with SWN) and conventional (n_c=1, no SWN) MMI crossings. The cross-talk measured from a vertical waveguide in the middle of the grid (the 51th waveguide) for index-engineered structure is also shown in Figure 6.

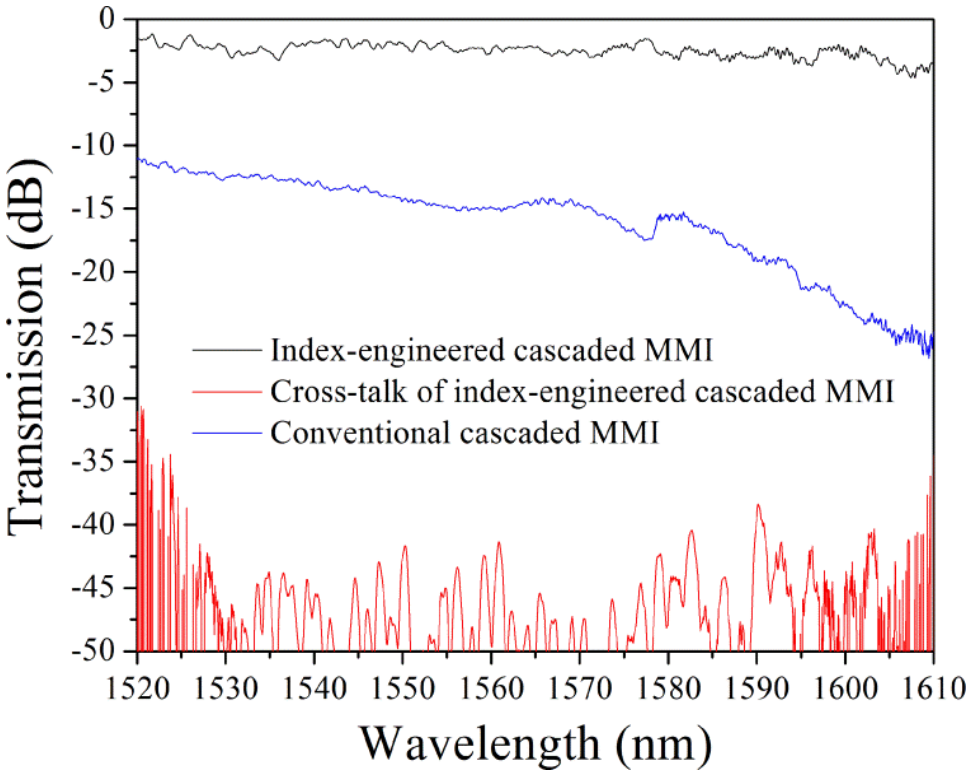

Figure 6-6: Measured transmission for 101 cascaded MMI crossings with (black) and without (blue) index-engineering, and the cross-talk of index-engineered MMI crossing.

The results show that the conventional MMI crossing has an insertion loss of 0.14 dB at 1550 nm operating wavelength, which is comparable to what demonstrated in ref. [2]. The index-engineered MMI crossing has an insertion loss of 0.019 dB at 1550 nm operating wavelength. The cross-talk signal is below the noise floor of our testing system, so the exact cross-talk cannot be extracted from the transmission. However, the real cross-talk is at least below -40 dB over 1530-1600 nm wavelength range. Besides the ultra-low insertion loss and low cross-talk, cascading index-engineered MMI crossings enable a waveguide pitch of 3.08 μm in a cross-grid, which is the most compact footprint for non-resonant crossings to our knowledge.

SUMMARY

In summary, an ultra-low loss waveguide crossing structure with a waveguide pitch of only 3.08 μm has been demonstrated on SOI platform. The crossing structure, utilizing cascaded index-engineered MMI, has insertion loss of 0.019 dB and crosstalk lower than -40 dB at 1550 nm operating wavelength, and broad transmission spectrum over more than 90 nm bandwidth.

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Chapter 7: Summary and Future Works

In this dissertation, three different approaches to build multi-layer single crystalline silicon based photonic integrated circuit (PIC) are demonstrated. In chapter 2, we showed that double-layer self-aligned waveguiding structure can be fabricated using only one lithography step and one etching step. Carefully optimized deep reactive ion etching (DRIE) was used to etch into commercially available double-bonded silicon-on-insulator (SOI) wafers to form photonic devices on both layers simultaneously. We designed, fabricated and characterized 1-to-12 fanouts using multi-mode interference (MMI) coupler on this platform, which showed low insertion loss and high uniformity on both layers. This platform, although benefit significantly from its simple fabrication process and large waveguide cross-sectional dimensions, which lead to low propagation loss and polarization independent operation, has several limitations: 1) the chip layout is restricted to self-aligned structure, and it is hard to integrated actively controlled devices into the bottom layer, 2) the large waveguide dimensions limit the possible bandwidth density, 3) the thickness variation in silicon layers results in effective refractive index variation, which is detrimental to index sensitive devices. Further investigation is required to integrate this platform into electronic chips.

As silicon nanomembrane with precise thickness control is strongly preferred for building silicon PICs, we developed a transfer printing technique to transfer large-area silicon nanomembranes, retrieved from SOI wafers, onto existing silicon PICs fabricated on SOI. Using to this method, we demonstrated the possibility to fabricate multi-layer PIC on vertically integrated silicon nanomembranes. Optical characterizations of 1-to-12 MMI couplers fabricated on the transfer printed silicon nanomembranes show encouraging results for further investigation. However, this approach has its limitations in

building chip-scale PICs: 1) the largest silicon nanomembrane that we successfully transferred is 8 mm X 2 mm, which is not large enough for on-chip optical interconnects applications, 2) the yield of transfer printing is limited, some defects are usually observed in the transfer printed silicon nanomembrane. A method to achieve larger and defect-free silicon nanomembrane is the first priority for optimizing this process.

In chapter 4, we demonstrated vertically integrated double-layer silicon nanomembrane platform using SU-8 based adhesive bonding and silicon handle removal. In this method, two SOI chips are bonded face-to-face using SU-8, and the silicon handle of one SOI chip is removed with mechanical polishing and DRIE. Silicon nanomembranes fabricated using this method are large and defect-free, and can be processed using standard lithography and etching. In order to couple light into this platform, we designed, fabricated and characterized fiber-to-chip grating couplers based on subwavelength nanostructures, which can simultaneously couple light into either of two silicon nanomembranes. The communication between two layers was also realized by using inter-layer grating couplers based on subwavelength nanostructures, which is the first demonstration of on-chip inter-layer light coupling on single crystalline silicon platform. The fabricated inter-layer grating coupler has a efficiency of 25% (-6.0 dB) and a 3 dB bandwidth of 41 nm. By using subwavelength nanostructures, we were able to pattern the grating couplers and waveguides at the same lithography step, which significantly simplifies the fabrication process.

With the fabrication method and grating couplers demonstrated in chapter 4, we were able to conveniently fabricate and characterize photonic devices fabricated on adhesively bonded silicon nanomembrane. In chapter 5, we designed, fabricated and characterized a 1-to-32 H-tree optical distribution network on adhesively bonded silicon nanomembrane. The single-mode waveguides fabricated on this platform has a

propagation loss of 4.3 dB/cm, which is comparable to waveguides fabricated on SOI. The H-tree structure has an excess loss of 2.2 dB, induced by Y-splitters, and output uniformity of 0.72 dB. This grating-coupled H-tree structure has a 3 dB bandwidth of 880 GHz measured by autocorrelation, which is sufficient to support the interconnect bandwidth requirement in future VLSI chips.

In order to further increase the potential bandwidth denstity and design flexibility in silicon membrane based PIC, we demonstrated an ultra-low loss waveguide crossing structure using cascaded index-engineered MMI coupler. The loss mechanism in MMI based crossing structure was identified as the mode polarization mismatch between multi-mode waveguide and waveguide crossing section. We proposed that this loss can be significantly reduced by increase the lateral cladding refractive index. A theoretical crossing loss of 0.008 dB was predicted. The index-engineering can be done using subwavelength nanostructure, which does not require any additional lithography step. We fabricated a 101x101 cross-grid constituting of index-engineered MMI crossings, and we measured the crossing loss to be 0.019 dB per crossing, which is the lowest demonstrated crossing loss so far. This crossing structure also has lower than -40 dB cross-talk and wide transmission spectrum covering entire C-band and L-band, which is suitable for wavelength division multiplexing (WDM). Moreover, the cascaded MMI crossings can achieve a waveguide pitch of only 3.08μm, which is the most compact structure demonstrated so far.

The potential future works of this dissertation include three parts:

First, in this dissertation, adhesively bonded silicon nanomembrane was identified as a promising solution to build multi-layer PIC, and basic building blocks such as intra- and inter-layer grating couplers, H-tree optical distribution network and ultra-low loss waveguide crossing were successfully demonstrated. However, there is still some room to

further improve the device performance. The intra- and inter-layer grating couplers can be re-optimized using the method described in ref. [1] to significantly improve the coupling efficiency. The waveguide propagation loss can be further reduced by replacing reactive ion etching (RIE) with inductively coupled plasma (ICP) etching. With these improvements, large-scale optical distribution can be realized in a multi-layer structure.

Second, the demonstrated low-temperature bonding method can be used to integrate multiple silicon photonic layers into the CMOS back-end process. Passive waveguiding structures demonstrated in this dissertation can be integrated with state-of-art active silicon photonic devices, such as modulators and photodetectors, to achieve the transmitting and receiving of optical signals at high data rates in a 3D PIC.

At last, this multi-layer silicon nanomembrane platform can be used for other applications, such as 3D optical phased array (OPA) [2].

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